Bicmos Technology And Applications 2nd Edition The Springer International Series In Engineering And Computer Science

' A reprint of the classic text, this book popularized compact modeling of electronic and semiconductor devices and components for college and graduate-school classrooms, and manufacturing engineering, over a decade ago. The first comprehensive book on MOS transistor compact modeling, it was the most cited among similar books in the area and remains the most frequently cited today. The coverage is device-physics based and continues to be relevant to the latest advances in MOS transistor modeling. This is also the only book that discusses in detail how to measure device model parameters required for circuit simulations. The book deals with the MOS Field Effect Transistor (MOSFET) models that are derived from basic semiconductor theory. Various models are developed, ranging from simple to more sophisticated models that take into account new physical effects observed in submicron transistors used in today''s (1993) MOS VLSI technology. The assumptions used to arrive at the models are emphasized so that the accuracy of the models in describing the device characteristics are clearly understood. Due to the importance of designing reliable circuits, device reliability models are also covered. Understanding these models is essential when designing circuits for state-of-the-art MOS ICs. Contents: OverviewReview of Basic Semiconductor and pn Junction TheoryMOS Transistor Structure and OperationMOS CapacitorThreshold VoltageMOSFET DC ModelDynamic ModelModeling Hot-Carrier EffectsData Acquisition and Model Parameter MeasurementsModel Parameter Extraction Using Optimization MethodSPICE Diode and MOSFET Models and Their ParametersStatistical Modeling and Worst-Case Design Parameters Readership: Integrated circuit chip designers, device model developers and circuit simulators. '

Timing research in high performance VLSI systems has advanced at a steady pace over the last few years, while tools, especially theoretical mechanisms, lag behind. Much present timing research relies heavily on timing diagrams, which, although intuitive, are inadequate for analysis of large designs with many parameters. Further, timing diagrams offer only approximations, not exact solutions, to many timing problems and provide little insight in the cases where temporal properties of a design interact intricately with the design's logical functionalities. This book presents a methodology for timing research which facilitates analy sis and design of circuits and systems in a unified temporal and logical domain. In the first part, we introduce an algebraic representation formalism, Timed Boolean Functions (TBF's), which integrates both logical and timing informa tion of digital circuits and systems into a single formalism. We also give a canonical form, TBF BDD's, for them, which can be used for efficient ma nipulation. In the second part, we apply Timed Boolean Functions to three problems in timing research, for which exact solutions are obtained for the first time: 1. computing the exact delays of combinational circuits and the minimum cycle times of finite state machines, 2. analysis and synthesis of wavepipelining circuits, a high speed architecture for which precise timing relations between signals are essential for correct operations, 3. verification of circuit and system performance and coverage of delay faults by testing.

It was about 1985 when both of the authors started their work using multigrid methods for process simulation problems. This happened in dependent from each other, with a completely different background and different intentions in mind. At this time, some important monographs appeared or have been in preparation. There are the three "classical" ones, from our point of view: the so-called "1984 Guide" [12J by Brandt, the "Multi-Grid Methods and Applications" [49J by Hackbusch and the so-called "Fundamentals" [132J by Stiiben and Trottenberg. Stiiben and Trottenberg in [132J state a "delayed acceptance, resent ments" with respect to multigrid algorithms. They complain: "Nevertheless, even today's situation is still unsatisfactory in several respects. If this is true for the development of standard methods, it applies all the more to the area of really difficult, complex applications." In spite of all the above mentioned publications and without ignoring important theoretical and practical improvements of multigrid, this situa tion has not yet changed dramatically. This statement is made under the condition that a numerical principle like multigrid is "accepted", if there exist "professional" programs for research and production purposes. "Professional" in this context stands for "solving complex technical prob lems in an industrial environment by a large community of users". Such a use demands not only for fast solution methods but also requires a high robustness with respect to the physical parameters of the problem.

Adaptive filtering is commonly used in many communication applications including speech and video predictive coding, mobile radio, ISDN subscriber loops, and multimedia systems. Existing adaptive filtering topologies are non-concurrent and cannot be pipelined. Pipelined Adaptive Digital Filters presents new pipelined topologies which are useful in reducing area and power and in increasing speed. If the adaptive filter portion of a system suffers from a power-speed-area bottleneck, a solution is provided. Pipelined Adaptive Digital Filters is required reading for all users of adaptive digital filtering algorithms. Algorithm, application and integrated circuit chip designers can learn how their algorithms can be tailored and implemented with lower area and power consumption and with higher speed. The relaxed look-ahead techniques are used to design families of new topologies for many adaptive filtering applications including least mean square and lattice adaptive filters, adaptive differential pulse code modulation coders, adaptive differential vector quantizers, adaptive decision feedback equalizers and adaptive Kalman filters. Those who use adaptive filtering in communications, signal and image processing algorithms can learn the basis of relaxed look-ahead pipelining and can use their own relaxations to design pipelined topologies suitable for their applications. Pipelined Adaptive Digital Filters is especially useful to designers of communications, speech, and video applications who deal with adaptive filtering, those involved with design of modems, wireless systems, subscriber loops, beam formers, and system identification applications. This book can also be used as a text for advanced courses on the topic.

Since the early 1980s, CAD frameworks have received a great deal of attention, both in the research community and in the commercial arena. It is generally agreed that CAD framework technology promises much: advanced CAD frameworks can turn collections of individual tools into effective and user-friendly design environments. But how can this promise be fulfilled? CAD Frameworks: Principles and Architecture describes the design and construction of CAD frameworks. It presents principles for building integrated design environments and shows how a CAD framework can be based on these principles. It derives the architecture of a CAD framework in a systematic way, using well-defined primitives for representation. This architecture defines how the many different framework sub-topics, ranging from concurrency control to design flow management, relate to each other and come together into an overall system. The origin of this work is the research and development performed in the context of the Nelsis CAD Framework, which has been a working system for well over eight years, gaining functionality while evolving from one

release to the next. The principles and concepts presented in this book have been field-tested in the Nelsis CAD Framework. CAD Frameworks: Principles and Architecture is primarily intended for EDA professionals, both in industry and in academia, but is also valuable outside the domain of electronic design. Many of the principles and concepts presented are also applicable to other design-oriented application domains, such as mechanical design or computer-aided software engineering (CASE). It is thus a valuable reference for all those involved in computer-aided design.

Low Voltage, Low Power

Digit-Serial Computation

SiGe and Si Strained-Layer Epitaxy for Silicon Heterostructure Devices

Materials, Fabrication, Devices, Circuits and Applications of SiGe and Si Strained-Layer Epitaxy

Connectionist Speech Recognition

Millimeter-Wave Antennas: Configurations and Applications

This book describes the newest implementations of integrated photodiodes fabricated in nanometer standard CMOS technologies. It also includes the required fundamentals, the state-of-the-art, and the design of high-performance laser drivers, transimpedance amplifiers, equalizers, and limiting amplifiers fabricated in nanometer CMOS technologies. This book shows the newest results for the performance of integrated optical receivers, laser drivers, modulator drivers and optical sensors in nanometer standard CMOS technologies. Nanometer CMOS technologies rapidly advanced, enabling the implementation of integrated optical receivers for high data rates of several Giga-bits per second and of high-pixel count optical imagers and sensors. In particular, low cost silicon CMOS optoelectronic integrated circuits became very attractive because they can be extensively applied to short-distance optical communications, such as local area network, chip-to-chip and board-to-board interconnects as well as to imaging and medical sensors.

PLEASE PROVIDE COURSE INFORMATION PLEASE PROVIDE

Mixed-Mode Simulation and Analog Multilevel Simulation addresses the problems of simulating entire mixed analog/digital systems in the time-domain. A complete hierarchy of modeling and simulation methods for analog and digital circuits is described. Mixed-Mode Simulation and Analog Multilevel Simulation also provides a chronology of the research in the field of mixed-mode simulation and analog multilevel simulation over the last ten to fifteen years. In addition, it provides enough information to the reader so that a prototype mixed-mode simulator could be developed using the algorithms in this book. Mixed-Mode Simulation and Analog Multilevel Simulation can also be used as documentation for the SPLICE family of mixed-mode programs as they are based on the algorithms and techniques described in this book.

An Analog VLSI System for Stereoscopic Vision investigates the interaction of the physical medium and the computation in both biological and analog VLSI systems by synthesizing a functional neuromorphic system in silicon. In both the synthesis and analysis of the system, a point of view from within the system is adopted rather than that of an omniscient designer drawing a blueprint. This perspective projects the design and the designer into a living landscape. The motivation for a machine-centered perspective is explained in the first chapter. The second chapter describes the evolution of the silicon retina. The retina accurately encodes visual information over orders of magnitude of ambient illumination, using mismatched components that are calibrated as part of the encoding process. The visual abstraction created by the retina is suitable for transmission through a limited bandwidth channel. The third chapter introduces a general method for interchip communication, the address-event representation, which is used for transmission of retinal data. The address-event representation takes advantage of the speed of CMOS relative to biological neurons to preserve the information of biological action potentials using digital circuitry in place of axons. The fourth chapter describes a collective circuit that computes stereodisparity. In this circuit, the processing that corrects for imperfections in the hardware compensates for inherent ambiguity in the environment. The fifth chapter demonstrates a primitive working stereovision system. An Analog VLSI System for Stereoscopic Vision contributes to both computer engineering and neuroscience at a concrete level. Through the construction of a working analog of biological vision subsystems, new circuits for building brain-style analog computers have been developed. Specific neuropysiological and psychophysical results in terms of underlying electronic mechanisms are explained. These examples demonstrate the utility of using biological principles for building brain-style computers and the significance of building brain-style computers for understanding the nervous system.

BiCMOS Technology and Applications, Second Edition provides a synthesis of available knowledge about the combination of bipolar and MOS transistors in a common integrated circuit - BiCMOS. In this new edition all chapters have been updated and completely new chapters on emerging topics have been added. In addition, BiCMOS Technology and Applications, Second Edition provides the reader with a knowledge of either CMOS or Bipolar technology/design a reference with which they can make educated decisions regarding the viability of BiCMOS in their own application. BiCMOS Technology and Applications, Second Edition is vital reading for practicing integrated circuit engineers as well as technical managers trying to evaluate business issues related to BiCMOS. As a textbook, this book is also appropriate at the graduate level for a special topics course in BiCMOS. A general knowledge in device physics, processing and circuit design is assumed. Given the division of the book, it lends itself well to a two-part course; one on technology and one on design. This will provide advanced students with a good understanding of tradeoffs between bipolar and MOS devices and circuits.

Mixed-Mode Simulation and Analog Multilevel Simulation

Asymptotic Waveform Evaluation

Analog Device-Level Layout Automation

Silicon Heterostructure Devices

Silicon Heterostructure Handbook

Robustness in Automatic Speech Recognition

This book comprehensively reviews the state of the art in millimeter-wave antennas, traces important recent developments and provides information on a wide range of antenna configurations and applications. While fundamental theoretical aspects are discussed whenever necessary, the book primarily focuses on design principles and concepts, manufacture, measurement techniques, and practical results. Each of the various antenna types scalable to millimeter-wave dimensions is considered individually, with coverage of leaky-wave and surface-wave antennas, printed antennas, integrated antennas, and reflector and lens systems. The final two chapters address the subject from a systems perspective, providing an overview of supporting circuitry and examining in detail diverse millimeter-wave applications, including high-speed wireless communications, radio astronomy, and radar. The vast amount of information now available on millimeter-wave systems can be daunting for researchers and designers entering the field. This book offers readers essential guidance, helping them to gain a thorough understanding based on the most recent research findings and serving as a sound basis for informed decision-making.

This proceedings volume archives the contributions of the speakers who attended the NATO Advanced Research Workshop on “Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment” held at the Sanatorium Puscha Ozerna, th th Kyiv, Ukraine, from 25 to 29 April 2004. The semiconductor industry has maintained a very rapid growth during the last three decades through impressive technological achievements which have resulted in products with higher performance and lower cost per function. After many years of development semiconductor-on-insulator materials have entered volume production and will increasingly be used by the manufacturing industry. The wider use of semiconductor (especially silicon) on insulator materials will not only enable the benefits of these materials to be further demonstrated but, also, will drive down the cost of substrates which, in turn, will stimulate the development of other novel devices and applications. In itself this trend will encourage the promotion of the skills and ideas generated by researchers in the Former Soviet Union and Eastern Europe and their incorporation in future collaborations.

The quest for higher performance digital systems for applications such as gen eral purpose computing, signal/image processing, and telecommunications and an increasing cost consciousness have led to a major thrust for high speed VLSI systems implemented in inexpensive and widely available technologies such as CMOS. This monograph, based on the first author's doctoral dissertation, con centrates on the technique of wave pipelining as one method toward achieving this goal. The primary focus of this monograph is to provide a coherent pre sentation of the theory of wave pipelined operation of digital circuits and to discuss practical design techniques for the realization of wave pipelined circuits in the CMOS technology. Wave pipelining can be applied to a variety of cir cuits for increased performance. For example, many architectures that support systolic computation lend themselves to wave pipelined realization. Also, the wave pipeline design methodology emphasizes the role of controlled clock skew in extracting enhanced performance from circuits that are not deeply pipelined. Wave pipelining (also known as maximal rate pipelining) is a timing method ology used in digital systems to increase the number of effective pipeline stages without increasing the number of physical registers in the pipeline. Using this technique, new data is applied to the inputs of a combinational logic block be fore the outputs due to previous inputs are available thus effectively pipelining the combinational logic and maximizing the utilization of the logic.

Designing VLSI systems represents a challenging task. It is a transfonnation among different specifications corresponding to different levels of design: abstraction, behavioral, stntctural and physical. The behavioral level describes the functionality of the design. It consists of two components; static and dynamic. The static component describes operations, whereas the dynamic component describes sequencing and timing. The structural level contains infonnation about components, control and connectivity. The physical level describes the constraints that should be imposed on the floor plan, the placement of components, and the geometry of the design. Constraints of area, speed and power are also applied at this level. To implement such multilevel transfonnation, a design methodology should be devised, taking into consideration the constraints, limitations and properties of each level. The mapping process between any of these domains is non-isomorphic. A single behavioral component may be transfonned into more than one structural component. Design methodologies are the most recent evolution in the design automation era, which started off with the introduction and subsequent usage of module generation especially for regular structures such as PLA's and memories. A design methodology should offer an integrated design system rather than a set of separate unrelated routines and tools. A general outline of a desired integrated design system is as follows: * Decide on a certain unified framework for all design levels. * Derive a design method based on this framework. * Create a design environment to implement this design method.

During the last decade, CMOS has become increasingly attractive as a basic integrated circuit technology due to its low power (at moderate frequencies), good scalability, and rail-to-rail operation. There are now a variety of CMOS circuit styles, some based on static complementary con ductance properties, but others borrowing from earlier NMOS techniques and the advantages of using clocking disciplines for precharge-evaluate se quencing. In this comprehensive book, the reader is led systematically through the entire range of CMOS circuit design. Starting with the in dividual MOSFET, basic circuit building blocks are described, leading to a broad view of both combinatorial and sequential circuits. Once these circuits are considered in the light of CMOS process technologies, impor tant topics in circuit performance are considered, including characteristics of interconnect, gate delay, device sizing, and I/O buffering. Basic circuits are then composed to form macro elements such as multipliers, where the reader acquires a unified view of architectural performance through par allelism, and circuit performance through careful attention to circuit-level and layout design optimization. Topics in analog circuit design reflect the growing tendency for both analog and digital circuit forms to be combined on the same chip, and a careful treatment of BiCMOS forms introduces the reader to the combination of both FET and bipolar technologies on the same chip to provide improved performance.

Wave Pipelining: Theory and CMOS Implementation

And Moment Matching for Interconnect Analysis

Circuits and Applications Using Silicon Heterostructure Devices
Multigrid Methods for Process Simulation
On Optimal Interconnections for VLSI
CMOS VLSI Engineering

BiCMOS Technology and ApplicationsSpringer Science & Business Media

When you see a nicely presented set of data, the natural response is: “How did they do that; what tricks did they use; and how can I do that for myself?” Alas, usually, you must simply keep wondering, since such tricks-of- the-trade are usually held close to the vest and rarely divulged. Shamefully ignored in the technical literature, measurement and modeling of high-speed semiconductor devices is a fine art. Robust measuring and modeling at the levels of performance found in modern SiGe devices requires extreme dexterity in the laboratory to obtain reliable data, and then a valid model to fit that data. Drawn from the comprehensive and well-reviewed Silicon Heterostructure Handbook, this volume focuses on measurement and modeling of high-speed silicon heterostructure devices. The chapter authors provide experience-based tricks-of-the-trade and the subtle nuances of measuring and modeling advanced devices, making this an important reference for the semiconductor industry. It includes easy-to-reference appendices covering topics such as the properties of silicon and germanium, the generalized Moll-Ross relations, the integral charge-control model, and sample SiGe HBT compact model parameters.
The book gives a comprehensive coverage of ICs and can be divided into three parts. The first deals with processing, component formation, and device modelling. The second part covers digital and analogue circuits, including semicondutor memories, with performance summaries of commercialproducts. The final part explains the nature of application specific integrated circuits (ASICs), and the ASIC design process. The final chapter covers VLSI scaling and the dominant role of interconnections in the scaling process. The text caters for many enginers and scientists who need to have agrasp of IC capabilities and ASIC design rooted in an appreciation of processing, device, behaviour, and circuit practice.
Silicon-On-Insulator (SOI) CMOS technology has been regarded as another major technology for VLSI in addition to bulk CMOS technology. Owing to the buried oxide structure, SOI technology offers superior CMOS devices with higher speed, high density, and reduced second order effects for deep-submicron low-voltage, low-power VLSI circuits applications. In addition to VLSI applications, and because of its outstanding properties, SOI technology has been used to realize communication circuits, microwave devices, BICMOS devices, and even fiber optics applications. CMOS VLSI Engineering: Silicon-On-Insulator addresses three key factors in engineering SOI CMOS VLSI - processing technology, device modelling, and circuit designs are all covered with their mutual interactions. Starting from the SOI CMOS processing technology and the SOI CMOS digital and analog circuits, behaviors of the SOI CMOS devices are presented, followed by a CAD program, ST-SPICE, which incorporates models for deep-submicron fully-depleted mesa-isolated SOI CMOS devices and special purpose SOI devices including polysilicon TFTs. CMOS VLSI Engineering: Silicon-On-Insulator is written for undergraduate senior students and first-year graduate students interested in CMOS VLSI. It will also be suitable for electrical engineering professionals interested in microelectronics.
For upper level and graduate level Electrical and Computer Engineering courses in Integrated Circuit Design as well as professional circuit designers, engineers and researchers working in portable wireless communications hardware. This book presents the fundamentals of Complementary Metal Oxide Semiconductor (CMOS) and Bipolar compatible Complementary Metal Oxide Semiconductor (BiCMOS) technology, as well as the latest technological advances in the field. It discusses the concepts and techniques of new integrated circuit design for building high performance and low power circuits and systems for current and future very-large-scale-integration (VLSI) and giga-scale-integration (GSI) applications. CMOS/BiCMOS ULSI: Low-Voltage Low-Power is an essential resource for every professional moving toward lower voltage, lower power, and higher performance VLSI circuits and subsystems design.

Fabrication of SiGe HBT BiCMOS Technology
Digital Timing Macromodeling for VLSI Design Verification
Integrated Circuit Engineering
MOSFET Models for VLSI Circuit Simulation
Low-voltage, Low-power Digital BiCMOS Circuits
Circuit Design, Comparative Study, and Sensitivity Analysis

Foreword Looking back the past 30 years. we have seen steady progress made in the area of speech science and technology. I still remember the excitement in the late seventies when Texas Instruments came up with a toy named "Speak-and-Spell" which was based on a VLSI chip containing the state-of-the-art linear prediction synthesizer. This caused a speech technology fever among the electronics industry. Particularly. applications of automatic speech recognition were rigorously attempt ed by many companies. some of which were start-ups founded just for this purpose. Unfortunately. it did not take long before they realized that automatic speech rec ognition technology was not mature enough to satisfy the need of customers. The fever gradually faded away. In the meantime. constant efforts have been made by many researchers and engi neers to improve the automatic speech recognition technology. Hardware capabilities have advanced impressively since that time. In the past few years. we have been witnessing and experiencing the advent of the "Information Revolution." What might be called the second surge of interest to com mercialize speech technology as a natural interface for man-machine communication began in much better shape than the first one. With computers much more powerful and faster. many applications look realistic this time. However. there are still tremendous practical issues to be overcome in order for speech to be truly the most natural interface between humans and machines.
Connectionist Speech Recognition: A Hybrid Approach describes the theory and implementation of a method to incorporate neural network approaches into state of the art continuous speech recognition systems

based on hidden Markov models (HMMs) to improve their performance. In this framework, neural networks (and in particular, multilayer perceptrons or MLPs) have been restricted to well-defined subtasks of the whole system, i.e. HMM emission probability estimation and feature extraction. The book describes a successful five-year international collaboration between the authors. The lessons learned form a case study that demonstrates how hybrid systems can be developed to combine neural networks with more traditional statistical approaches. The book illustrates both the advantages and limitations of neural networks in the framework of a statistical systems. Using standard databases and comparison with some conventional approaches, it is shown that MLP probability estimation can improve recognition performance. Other approaches are discussed, though there is no such unequivocal experimental result for these methods. Connectionist Speech Recognition is of use to anyone intending to use neural networks for speech recognition or within the framework provided by an existing successful statistical approach. This includes research and development groups working in the field of speech recognition, both with standard and neural network approaches, as well as other pattern recognition and/or neural network researchers. The book is also suitable as a text for advanced courses on neural networks or speech processing.

The topic of bipolar compatible CMOS (BiCMOS) is a fascinating one and of ever-growing practical importance. The "technology pendulum" has swung from the two extremes of preeminence of bipolar in the 1950s and 60s to the apparent endless horizons for VLSI NMOS technology during the 1970s and 80s. Yet starting in the 1980s severallimits were clouding the horizon for pure NMOS technology. CMOS reemerged as a· viable high density, high performance technology. Similarly by the mid 1980s scaled bipolar devices had not only demonstrated new high speed records, but early versions of mixed bipolar/CMOS technology were being produced. Hence the paradigm of either high density . Q[high speed was metamorphasizing into an opportunity for both speed and density via a BiCMOS approach. Now as we approach the 1990s there have been a number of practical demonstrations of BiCMOS both for memory and logic applications and I expect the trend to escalate over the next decade. This book makes a timely contribution to the field of BiCMOS technology and circuit development. The evolution is now indeed rapid so that it is difficult to make such a book exhaustive of current developments. Probably equally difficult is the fact that the new technology opens a range of novel circuit opportunities that are as yet only formative in their development. Given these obstacles it is a herculean task to try to assemble a book on BiCMOS.

No matter how you slice it, semiconductor devices power the communications revolution. Skeptical? Imagine for a moment that you could flip a switch and instantly remove all the integrated circuits from planet Earth. A moment’s reflection would convince you that there is not a single field of human endeavor that would not come to a grinding halt, be it commerce, agriculture, education, medicine, or entertainment. Life, as we have come to expect it, would simply cease to exist. Drawn from the comprehensive and well-reviewed Silicon Heterostructure Handbook, this volume covers SiGe circuit applications in the real world. Edited by John D. Cressler, with contributions from leading experts in the field, this book presents a broad overview of the merits of SiGe for emerging communications systems. Coverage spans new techniques for improved LNA design, RF to millimeter-wave IC design, SiGe MMICs, SiGe Millimeter-Wave ICs, and wireless building blocks using SiGe HBTs. The book provides a glimpse into the future, as envisioned by industry leaders.

This book provides a system-level approach to making packaging decisions for millimeter-wave transceivers. In electronics, the packaging forms a bridge between the integrated circuit or individual device and the rest of the electronic system, encompassing all technologies between the two. To be able to make well-founded packaging decisions, researchers need to understand a broad range of aspects, including: concepts of transmission bands, antennas and propagation, integrated and discrete package substrates, materials and technologies, interconnects, passive and active components, as well as the advantages and disadvantages of various packages and packaging approaches, and package-level modeling and simulation. Packaging also needs to be considered in terms of system-level testing, as well as associated testing and production costs, and reducing costs. This peer-reviewed work contributes to the extant scholarly literature by addressing the aforementioned concepts and applying them to the context of the millimeter-wave regime and the unique opportunities that this transmission approach offers.

Theory and Practice

A Hybrid Approach

Measurement and Modeling of Silicon Heterostructure Devices

Simulation Techniques and Solutions for Mixed-Signal Coupling in Integrated Circuits

Modern Methods of Speech Processing

Optoelectronic Circuits in Nanometer CMOS Technology

As their name implies, VLSI systems involve the integration of various component systems. While all of these components systems are rooted in semiconductor manufacturing, they involve a broad range of technologies. This volume of the Principles and Applications of Engineering series examines the technologies associated with VLSI systems, including

The term speech processing refers to the scientific discipline concerned with the analysis and processing of speech signals for getting the best benefit in various practical scenarios. These different practical scenarios correspond to a large variety of applications of speech processing research. Examples of some applications include enhancement, coding, synthesis, recognition and speaker recognition. A very rapid growth, particularly during the past ten years, has resulted due to the efforts of many leading scientists. The ideal aim is to develop algorithms for a certain task that maximize performance, are computationally feasible and are robust to a wide class of conditions. The purpose of this book is to provide a cohesive collection of articles that describe recent advances in various branches of speech processing. The main focus is in describing specific research directions through a detailed analysis and review of both the theoretical and practical settings. The intended audience includes graduate students who are embarking on speech research as well as the experienced researcher already working in the field. For graduate students taking a course, this book serves as a supplement to the course material. As the student focuses on a particular topic, the corresponding set of articles in this book will serve as an initiation through exposure to research issues and by providing an extensive reference list to commence a literature survey. Expe rienced researchers can utilize this book as a reference guide and can expand their horizons in this rather broad area.

On Optimal Interconnections for VLSI describes, from a geometric perspective, algorithms for high-performance, high-density interconnections during the global and detailed routing phases of circuit layout. First, the book addresses area minimization, with a focus on near-optimal approximation algorithms for minimum-cost Steiner routing. In addition to practical implementations of recent methods, the implications of recent results on spanning tree degree bounds and the method of Zelikovsky are discussed. Second, the book addresses delay minimization, starting with a discussion of accurate, yet

algorithmically tractable, delay models. Recent minimum-delay constructions are highlighted, including provably good cost-radius tradeoffs, critical-sink routing algorithms, Elmore delay-optimal routing, graph Steiner arborescences, non-tree routing, and wiresizing. Third, the book addresses skew minimization for clock routing and prescribed-delay routing formulations. The discussion starts with early matching-based constructions and goes on to treat zero-skew routing with provably minimum wirelength, as well as planar clock routing. Finally, the book concludes with a discussion of multiple (competing) objectives, i.e., how to optimize area, delay, skew, and other objectives simultaneously. These techniques are useful when the routing instance has heterogeneous resources or is highly congested, as in FPGA routing, multi-chip packaging, and very dense layouts. Throughout the book, the emphasis is on practical algorithms and a complete self-contained development. On Optimal Interconnections for VLSI will be of use to both circuit designers (CAD tool users) as well as researchers and developers in the area of performance-driven physical design.

Modern microelectronic design is characterized by the integration of full systems on a single die. These systems often include large high performance digital circuitry, high resolution analog parts, high driving I/O, and maybe RF sections. Designers of such systems are constantly faced with the challenge to achieve compatibility in electrical characteristics of every section: some circuitry presents fast transients and large consumption spikes, whereas others require quiet environments to achieve resolutions well beyond millivolts. Coupling between those sections is usually unavoidable, since the entire system shares the same silicon substrate bulk and the same package. Understanding the way coupling is produced, and knowing methods to isolate coupled circuitry, and how to apply every method, is then mandatory knowledge for every IC designer. Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs is an in-depth look at coupling through the common silicon substrate, and noise at the power supply lines. It explains the elementary knowledge needed to understand these phenomena and presents a review of previous works and new research results. The aim is to provide an understanding of the reasons for these particular ways of coupling, review and suggest solutions to noise coupling, and provide criteria to apply noise reduction. Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs is an ideal book, both as introductory material to noise-coupling problems in mixed-signal ICs, and for more advanced designers facing this problem.

What seems routine today was not always so. The field of Si-based heterostructures rests solidly on the shoulders of materials scientists and crystal growers, those purveyors of the semiconductor “ black arts ” associated with the deposition of pristine films of nanoscale dimensionality onto enormous Si wafers with near infinite precision. We can now grow near-defect free, nanoscale films of Si and SiGe strained-layer epitaxy compatible with conventional high-volume silicon integrated circuit manufacturing. SiGe and Si Strained-Layer Epitaxy for Silicon Heterostructure Devices tells the materials side of the story and details the many advances in the Si-SiGe strained-layer epitaxy for device applications. Drawn from the comprehensive and well-reviewed Silicon Heterostructure Handbook, this volume defines and details the many advances in the Si/SiGe strained-layer epitaxy for device applications. Mining the talents of an international panel of experts, the book covers modern SiGe epitaxial growth techniques, epi defects and dopant diffusion in thin films, stability constraints, and electronic properties of SiGe, strained Si, and Si-C alloys. It includes appendices on topics such as the properties of Si and Ge, the generalized Moll-Ross relations, integral charge-control relations, and sample SiGe HBT compact model parameters.

VLSI Technology
Fundamentals of Solid State Electronics
Systems-Level Packaging for Millimeter-Wave Transceivers
Silicon-on-Insulator (SOI)
Pipelined Adaptive Digital Filters
Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs

This is perhaps the most comprehensive undergraduate textbook on the fundamental aspects of solid state electronics. It presents basic and state-of-the-art topics on materials physics, device physics, and basic circuit building blocks not covered by existing textbooks on the subject. Each topic is introduced with a historical background and motivations of device invention and circuit evolution. Fundamental physics is rigorously discussed with minimum need of tedious algebra and advanced mathematics. Another special feature is a systematic classification of fundamental mechanisms not found even in advanced texts. It bridges the gap between solid state device physics covered here with what students have learnt in their first two years of study. Used very successfully in a one-semester introductory core course for electrical and other engineering, materials science and physics junior students, the second part of each chapter is also used in an advanced undergraduate course on solid state devices. The inclusion of previously unavailable analyses of the basic transistor digital circuit building blocks and cells makes this an excellent reference for engineers to look up fundamental concepts and data, design formulae, and latest devices such as the GeSi heterostructure bipolar transistors. This book is also available as a set with Fundamentals of Solid-State Electronics — Study Guide and Fundamentals of Solid-State Electronics — Solution Manual.

The goal of putting `systems on a chip' has been a difficult challenge that is only recently being met. Since the world is `analog', putting systems on a chip requires putting analog interfaces on the same chip as digital processing functions. Since some processing functions are accomplished more efficiently in analog circuitry, chips with a large amount of analog and digital circuitry are being designed. Whether a small amount of analog circuitry is combined with varying amounts of digital circuitry or the other way around, the problem encountered in marrying analog and digital circuitry are the same but with different scope. Some of the most prevalent problems are chip/package capacitive and inductive coupling, ringing on the RLC tuned circuits that form the chip/package power supply rails and off-chip drivers and receivers, coupling between circuits through the chip substrate bulk, and radiated emissions from the chip/package interconnects. To aggravate the problems of designers who have to deal with the complexity of mixed-signal coupling there is a lack of verification techniques to simulate the problem. In addition to considering RLC models for the various chip/package/board level parasitics, mixed-signal circuit designers must also model coupling through the common substrate when simulating ICs to obtain an accurate estimate of coupled noise in their designs. Unfortunately, accurate simulation of substrate coupling has only recently begun to receive attention, and techniques for the same are not widely known. Simulation Techniques and Solutions for Mixed-Signal

Coupling in Integrated Circuits addresses two major issues of the mixed-signal coupling problem -- how to simulate it and how to overcome it. It identifies some of the problems that will be encountered, gives examples of actual hardware experiences, offers simulation techniques, and suggests possible solutions. Readers of this book should come away with a clear directive to simulate their design for interactions prior to building the design, versus a `build it and see' mentality.

The intense drive for signal integrity has been at the forefront ofrapid and new developments in CAD algorithms. Thousands ofengineers, intent on achieving the best design possible, use SPICE on a daily basis for analog simulation and general circuit analysis. But the strained demand for high data speeds, coupled with miniaturizationon an unprecedented scale, has highlighted the previously negligible effects of interconnects; effects which are not always handled appro priately by the present levels of SPICE. Signals at these higher speeds may be degraded by long interconnect lengths compared to the increasingly shorter sig nal rise times. Interconnect structures can be diverse (pins, connectors, leads, microstrips, striplines, etc.) and present at any of the hierarchical packaging levels: integrated circuits, printed circuit boards, multi-chip modules or sys tem backplanes. Analysis of these effects in any CAD package has become a necessity. Asymptotic waveform evaluation (AWE) and other moment matching tech niques have recently proven useful in the analysis of interconnect structures and various networks containing large linear structures with nonlinear termi nations. Previously, all that was available to the designer was a full SPICE simulation or a quick but uncertain timing estimation. Moment matching, used in linear systems analysis as a method of model reduction, describes a method to extract a small set of dominant poles from a large network. The information is obtained from the Taylor series coefficients (moments) of that system.

SiGe HBTs are the most mature of the Si heterostructure devices and not surprisingly the most completely researched and discussed in the technical literature. However, new effects and nuances of device operation are uncovered year-after-year as transistor scaling advances and application targets march steadily upward in frequency and sophistication. Providing a comprehensive treatment of SiGe HBTs, Silicon Heterostructure Devices covers an amazingly diverse set of topics, ranging from basic transistor physics to noise, radiation effects, reliability, and TCAD simulation. Drawn from the comprehensive and well-reviewed Silicon Heterostructure Handbook, this text explores SiGe heterojunction bipolar transistors (HBTs), heterostructure FETs, various other heterostructure devices, as well as optoelectronic components. The book provides an overview, characteristics, and derivative applications for each device covered. It discusses device physics, broadband noise, performance limits, reliability, engineered substrates, and self-assembling nanostructures. Coverage of optoelectronic devices includes Si/SiGe LEDs, near-infrared detectors, photonic transistors for integrated optoelectronics, and quantum cascade emitters. In addition to this substantial collection of material, the book concludes with a look at the ultimate limits of SiGe HBTs scaling. It contains easy-to-reference appendices on topics including the properties of silicon and germanium, the generalized Moll-Ross relations, and the integral charge-control model, and sample SiGe HBT compact model parameters.

Digital Timing Macromodeling for VLSI Design Verification first of all provides an extensive history of the development of simulation techniques. It presents detailed discussion of the various techniques implemented in circuit, timing, fast-timing, switch-level timing, switch-level, and gate-level simulation. It also discusses mixed-mode simulation and interconnection analysis methods. The review in Chapter 2 gives an understanding of the advantages and disadvantages of the many techniques applied in modern digital macromodels. The book also presents a wide variety of techniques for performing nonlinear macromodeling of digital MOS subcircuits which address a large number of shortcomings in existing digital MOS macromodels. Specifically, the techniques address the device model detail, transistor coupling capacitance, effective channel length modulation, series transistor reduction, effective transconductance, input terminal dependence, gate parasitic capacitance, the body effect, the impact of parasitic RC-interconnects, and the effect of transmission gates. The techniques address major sources of errors in existing macromodeling techniques, which must be addressed if macromodeling is to be accepted in commercial CAD tools by chip designers. The techniques presented in Chapters 4-6 can be implemented in other macromodels, and are demonstrated using the macromodel presented in Chapter 3. The new techniques are validated over an extremely wide range of operating conditions: much wider than has been presented for previous macromodels, thus demonstrating the wide range of applicability of these techniques.

A Unified Approach for Microelectronics Systems Manufacturing & Software Development

BiCMOS Technology and Applications

CMOS/BiCMOS ULSI

Establishing a Foundation

Timed Boolean Functions

SiGe HBT BiCMOS technology is the obvious groundbreaker of the Si heterostructures application space. To date virtually every major player in the communications electronics market either has SiGe up and running in-house or is using someone else ' s SiGe fab as foundry for their designers. Key to this success lies in successful integration of the SiGe HBT and Si CMOS, with no loss of performance from either device. Filled with contributions from leading experts, Fabrication of SiGe HBT BiCMOS Technologies brings together a complete discussion of these topics into a single resource. Drawn from the comprehensive and well-reviewed Silicon Heterostructure Handbook, this volume examines the design, fabrication, and application of silicon heterostructure transistors. A novel aspect of this book the inclusion of numerous snapshot views of the industrial state-of-the-art for SiGe HBT BiCMOS technology. It has been carefully designed to provide a useful basis of comparison for the current status and future course of the global industry. In addition to the copious technical material and the numerous references contained in each chapter, the book includes easy-to-reference appendices on the properties of Si and Ge, the generalized Moll-Ross relations, integral charge-control relations, and sample SiGe HBT compact model parameters.

The international market is very competitive for high-tech manufacturers to day. Achieving competitive quality and reliability for products requires leader ship from the top, good management practices, effective and efficient operation and maintenance systems, and use of appropriate up-to-date engineering de sign tools and methods. Furthermore, manufacturing yield and reliability are interrelated. Manufacturing yield depends on the number of defects found dur ing both the manufacturing process and the warranty period, which in turn determines the reliability. the production of microelectronics has evolved into Since the early 1970's, one of the world's largest manufacturing industries. As a result, an important agenda is the study of reliability issues in

fabricating microelectronic products and consequently the systems that employ these products, particularly, the new generation of microelectronics. Such an agenda should include: • the economic impact of employing the microelectronics fabricated by in dustry, • a study of the relationship between reliability and yield, • the progression toward miniaturization and higher reliability, and • the correctness and complexity of new system designs, which include a very significant portion of software.

This book presents a detailed summary of research on automatic layout of device-level analog circuits that was undertaken in the late 1980s and early 1990s at Carnegie Mellon University. We focus on the work behind the creation of the tools called KOAN and ANAGRAM II, which form part of the core of the CMU ACACIA analog CAD system. KOAN is a device placer for custom analog cells; ANANGRAM II a detailed area router for these analog cells. We strive to present the motivations behind the architecture of these tools, including detailed discussion of the subtle technology and circuit concerns that must be addressed in any successful analog or mixed-signal layout tool. Our approach in organizing the chapters of the book has been to present our algo rithms as a series of responses to these very real and very difficult analog layout problems. Finally, we present numerous examples of results generated by our algorithms. This research was supported in part by the Semiconductor Research Corpora tion, by the National Science Foundation, by Harris Semiconductor, and by the International Business Machines Corporation Resident Study Program. Finally, just for the record: John Cohn was the designer of the KOAN placer; David Garrod was the designer of the ANAGRAM II router (and its predeces sor, ANAGRAM I). This book was architected by all four authors, edited by John Cohn and Rob Rutenbar, and produced in finished form by John Cohn.

An extraordinary combination of material science, manufacturing processes, and innovative thinking spurred the development of SiGe heterojunction devices that offer a wide array of functions, unprecedented levels of performance, and low manufacturing costs. While there are many books on specific aspects of Si heterostructures, the Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits, and Applications of SiGe and Si Strained-Layer Epitaxy is the first book to bring all aspects together in a single source. Featuring broad, comprehensive, and in-depth discussion, this handbook distills the current state of the field in areas ranging from materials to fabrication, devices, CAD, circuits, and applications. The editor includes "snapshots" of the industrial state-of-the-art for devices and circuits, presenting a novel perspective for comparing the present status with future directions in the field. With each chapter contributed by expert authors from leading industrial and research institutions worldwide, the book is unequalled not only in breadth of scope, but also in depth of coverage, timeliness of results, and authority of references. It also includes a foreword by Dr. Bernard S. Meyerson, a pioneer in SiGe technology. Containing nearly 1000 figures along with valuable appendices, the Silicon Heterostructure Handbook authoritatively surveys materials, fabrication, device physics, transistor optimization, optoelectronics components, measurement, compact modeling, circuit design, and device simulation.

Digital signal processing (DSP) is used in a wide range of applications such as speech, telephone, mobile radio, video, radar and sonar. The sample rate requirements of these applications range from 10 KHz to 100 MHz. Real time implementation of these systems requires design of hardware which can process signal samples as these are received from the source, as opposed to storing them in buffers and processing them in batch mode. Efficient implementation of real time hardware for DSP applications requires study of families of architectures and implementation styles out of which an appropriate architecture can be selected for a specified application. To this end, the digit-serial implementation style is proposed as an appropriate design methodology for cases where bit-serial systems cannot meet the sample rate requirements, and bit-parallel systems require excessive hardware. The number of bits processed in a clock cycle is referred to as the digit-size. The hardware complexity and the achievable sample rate increase with increase in the digit-size. As special cases, a digit serial system is reduced to bit-serial or bit-parallel when the digit-size is selected to equal one or the word-length, respectively. A family of implementations can be obtained by changing the digit-size parameter, thus permitting an optimal trade-off between throughput and size. Because of their structured architecture, digit-serial designs lend themselves to automatic compilation from algorithmic descriptions. An implementation of this design methodology, the Parsifal silicon compiler was developed at the General Electric Corporate Research and Development laboratory.

Circuit Design for CMOS VLSI

Cad Frameworks

Proceedings of the NATO Advanced Research Workshop on Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment, Kiev, Ukraine, 26-30 April 2004

Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment

A Unified Formalism for Exact Timing Analysis

Principles and Architecture

Metal Oxide Semiconductor (MOS) transistors are the basic building block ofMOS integrated circuits (I C). Very Large Scale Integrated (VLSI) circuits using MOS technology have emerged as the dominant technology in the semiconductor industry. Over the past decade, the complexity of MOS IC's has increased at an astonishing rate. This is realized mainly through the reduction of MOS transistor dimensions in addition to the improvements in processing. Today VLSI circuits with over 3 million transistors on a chip, with effective or electrical channel lengths of 0. 5 microns, are in volume production. Designing such complex chips is virtually impossible without simulation tools which help to predict circuit behavior before actual circuits are fabricated. However, the utility of simulators as a tool for the design and analysis of circuits depends on the adequacy of the device models used in the simulator. This problem is further aggravated by the technology trend towards smaller and smaller device dimensions which increases the complexity of the models. There is extensive literature available on modeling these short channel devices. However, there is a lot of confusion too. Often it is not clear what model to use and which model parameter values are important and how to determine them. After working over 15 years in the field of semiconductor device modeling, I have felt the

need for a book which can fill the gap between the theory and the practice of MOS transistor modeling. This book is an attempt in that direction.

VLSI Design Methodologies for Digital Signal Processing Architectures

An Analog VLSI System for Stereoscopic Vision

Reliability, Yield, and Stress Burn-In

Fundamentals and Applications

Mosfet Modeling for VLSI Simulation