Burn In Test Socket Workshop

MCMs today consist of complex and dense VLSI devices mounted into packages that allow little physical access to internal nodes. The complexity and cost associated with their test and diagnosis are major obstacles to their use. Multi-Chip Module Test Strategies presents state-of-the-art test strategies for MCMs. This volume of original research is designed for engineers interested in practical implementations of MCM test solutions and for designers looking for leading edge test and design-for-testability solutions for their next designs. Multi-Chip Module Test Strategies consists of eight contributions by leading researchers. It is designed to provide a comprehensive and well-balanced coverage of the MCM test domain. Multi-Chip Module Test Strategies has also been published as a special issue of the Journal of Electronic Testing: Theory and Applications (JETTA, Volume 10, Numbers 1 and 2).

."... 10th anniversary of the Workshop ..."--P. x.

Proceedings

25-28 April 2000, the Adam's Mark Hotel, Denver, Colorado, USA

On-Line Testing Symposium, 2003. IOLTS 2003. 9th IEEE

The 2004 Asian International Workshop on Advanced Reliability Modeling is a symposium for the dissemination of state-of-the-art research and the presentation of practice in reliability engineering and related issues in Asia. It brings together researchers, scientists and practitioners from Asian countries to discuss the state of research and practice in dealing with reliability issues at the system design (modeling) level, and to jointly formulate an agenda for future research in this engineering area. The proceedings cover all the key topics in reliability, maintainability and safety engineering, providing an in-depth presentation of theory and practice. The proceedings have been selected for coverage in: • Index to Scientific & Technical Proceedings® (ISTP® / ISI Proceedings) • Index to Scientific & Technical Proceedings (ISTP CDROM version / ISI Proceedings) • CC Proceedings — Engineering & Physical Sciences Contents: How Can We Estimate Software Reliability with a Continuous-State Software Reliability Model? (T Ando & T Dohi)Performing the Soft-Error Rate (SER) on a TDBI Chamber (V Chang & W T K Chien)Warranty and Imperfect Repairs (S Chukova & Y Hayakawa)Availability for a Repairable System with Finite Repairs (L Cui & J Li)Reliability of a Server System with Access Restriction (M Imaizumi et al.)Simulated Annealing Algorithm for Redundancy Optimization with Multiple Component Choices (H G Kim et al.)A Random Shock Model for a Continuously Deteriorating System (K E Lim et al.)Five Further Studies for Reliability Models (T Nakagawa)Computation Technology for Safety and Risk Assessment of Gas Pipeline Systems (V Seleznev & V Aleshin)Automatic Pattern Classification Reliability of the Digitized Mammographic Breast Density (T Sumimoto et al.)and other papers Readership: Graduate students, researchers and practitioners in

industrial engineering, computer engineering, systems engineering, business management and mathematics. Keywords:Reliability;Maintenance;Safety;Failure;Risk Assessment;Testing;Modeling;Probability & Statistics

This second edition of An Engineer's Guide to Automated Testing of High-Speed Interfaces provides updates to reflect current state-of-the-art high-speed digital testing with automated test equipment technology (ATE). Featuring clear examples, this one-stop reference covers all critical aspects of automated testing, including an introduction to high-speed digital basics, a discussion of industry standards, ATE and bench instrumentation for digital applications, and test and measurement techniques for characterization and production environment. Engineers learn how to apply automated test equipment for testing high-speed digital I/O interfaces and gain a better understanding of PCI-Express 4, 100Gb Ethernet, and MIPI while exploring the correlation between phase noise and jitter. This updated resource provides expanded material on 28/32 Gbps NRZ testing and wireless testing that are becoming increasingly more pertinent for future applications. This book explores the current trend of merging high-speed digital testing within the fields of photonic and wireless testing.

Multi-Chip Module Test Strategies

Advanced Packaging

IC Component Sockets

A broad and practical reference to IC socket technology The first and only comprehensive resource on IC (Integrated Circuit) socket technology, IC Component Sockets offers a complete overview of socket technology and design in order to provide engineers and their managers with a good understanding of these specialized technologies and the processes for evaluating them. The authors, both acknowledged experts in the field, address all relevant aspects of the subject-including materials, design, performance characteristics, failure modes and mechanisms, and qualification and reliability assessment-with emphasis on the technology's inherent advantages and challenges. Topics of interest include: * Socket design and contact technologies * Performance characteristics and material properties * Contact failure modes and mechanisms * Qualification testing conditions * Qualification sequences and setup * IEEE prediction methodology * Theoretical calculation of contact reliability Including a list of standards and specifications, this book is an important and timely resource for today's electronics engineers concerned with evaluating and perfecting socket design, manufacture, and use.

Advanced Packaging serves the semiconductor packaging, assembly and test industry. Strategically focused on emerging and leading-edge methods for manufacturing and use of advanced packages.

IEEE VLSI Test Symposium

Infrared Tools For Solar Antrophysics: What's Next? - Proceedings Of The Fifteenth National Solar Observatory/sacramento Peak Summer Workshop

Records of the 2002 IEEE International Workshop on Memory Technology, Design and Testing

Held in Guam in November of 2002, the symposium on the test technologies and research issues related to silicon chip production, resulted in the 74 papers presented here. The papers are organized into sections related to the symposium sessions on test generation, on-line testing, analog and mixed si

Synopses are presented of the six invited talks and two discussion periods of a meeting in which 65 engineers and scientists, representing 36 organizations from private industry and government, participated. Topics ranged from failure analysis and the nature of leaks to evaluations and intercomparisons of bubble, weight, helium, and radioisotope tests. Underlying many of the problems discussed is the lack of a technical basis for specifications on maximum allowable leak rates and contaminant levels; no data are available to relate leak rate to component life. Of concern is the proliferation of test conditions which has complicated testing and test intercomparison efforts, and has resulted, unwittingly, in testing devices to significantly different actual leak rate criteria. Water vapor, sealed-in and that which penetrates the package, is a contaminant of major concern and the difficulties of making sufficiently accurate measurements of water vapor were detailed. The control required in the materials and assembly process to avoid hermeticity failure and false leak indications in ceramic, dual in-line packages was discussed. Finally, the importance of performing some hermeticity tests at elevated temperatures was cited.

Thermal and Power Management of Integrated Circuits

IEEE International Reliability Physics Symposium Proceedings

ARPA/NBS Workshop II

In Thermal and Power Management of Integrated Circuits, power and thermal management issues in integrated circuits during normal operating conditions and stress operating conditions are addressed. Thermal management in VLSI circuits is becoming an integral part of the design, test, and manufacturing. Proper thermal management is the key to achieve high performance, quality and reliability. Performance and reliability of integrated circuits are strong functions of the junction temperature. A small increase in junction temperature may result in significant reduction in the device lifetime. This book reviews the significance of the junction temperature as a reliability measure under nominal and burn-in conditions. The latest research in the area of electro-thermal modeling of integrated circuits will also be presented. Recent models and associated CAD tools are covered and various techniques at the circuit and system levels are reviewed. Subsequently, the authors provide an insight into the concept of thermal runaway and how it may best be avoided. A section on low temperature operation of integrated circuits concludes the book. Collects 58 papers from the April/May 2001 symposium that explore new approaches in the testing of electronic circuits and systems. Key areas in testing are discussed, such as BIST, analog measurement, fault tolerance, diagnosis methods, scan chain design, memory test and diagnosis, and test data compression and compaction. Also on the program are sessions on emerging areas that are gaining prominence, including low power testing, testing high speed circuits on low cost testers, processor based self test techniques, and core- based system-on-chip testing. Some of the

topics are robust and low cost BIST architectures for sequential fault testing in datapath multipliers, a method for measuring the cycle-to-cycle period jitter of high-frequency clock signals, fault equivalence identification using redundancy information and static and dynamic extraction, and test scheduling for minimal energy consumption under power constraints. No subject index. c. Book News Inc.

Hermeticity Testing for Integrated Circuits

Advanced Reliability Modeling

A unique book that describes the practical processes necessary to achieve failure free equipment performance, for quality and reliability engineers, design, manufacturing process and environmental test engineers. This book studies the essential requirements for successful product life cycle management. It identifies key contributors to failure in product life cycle management and particular emphasis is placed upon the importance of thorough Manufacturing Process Capability reviews for both in-house and outsourced manufacturing strategies. The readers? attention is also drawn to the many hazards to which a new product is exposed from the commencement of manufacture through to end of life disposal. Revolutionary in focus, as it describes how to achieve failure free performance rather than how to predict an acceptable performance failure rate (reliability technology rather than reliability engineering) Author has over 40 years experience in the field, and the text is based on classroom tested notes from the reliability technology course he taught at Massachusetts Institute of Technology (MIT), USA Contains graphical interpretations of mathematical models together with diagrams, tables of physical constants, case studies and unique worked examples

Wafer-level testing refers to a critical process of subjecting integrated circuits and semiconductor devices to electrical testing while they are still in wafer form. Burn-in is a temperature/bias reliability stress test used in detecting and screening out potential early life device failures. This hands-on resource provides a comprehensive analysis of these methods, showing how wafer-level testing during burn-in (WLTBI) helps lower product cost in semiconductor manufacturing. Engineers learn how to implement the testing of integrated circuits at the wafer-level under various resource constraints. Moreover, this unique book helps practitioners address the issue of enabling next generation products with previous generation testers. Practitioners also find expert insights on current industry trends in WLTBI test solutions.

Proceedings : April 29-May 3, 2001, Marina Del Rey, California, USA

International Workshop on Electronic Design, Test and Applications

Reliability Technology

A collection of the 78 oral presentations and 24 poster papers from the January 2002 international workshop which brought together specialists from a broad area of electronic design, manufacturing, test, and advanced system applications in the hope that the conference would integrate design, test, and application as "cross- dependent" disciplines. The contributions are organized into sessions focusing on analog test, communications, digital signal processing and architectures, low to high level fault simulation and identification, high level design, memory, power issues in design and test, sensor and analog design, electrical engineering education, electromagnetics and control, fault-tolerant digital systems, image processing, robotics, submicron technology, test generation and compaction, and test techniques and methodologies. Annotation copyrighted by Book News Inc., Portland, OR

Proceedings of a spring 2000 symposium, highlighting novel ideas and approaches to current and future problems related to testing of electronic circuits and systems. Themes are microprocessor test/validation, low power BIST and scan, technology trends, scan- related approaches, defect-driven techniques, and system-on-chip test techniques. Other subjects are analog test techniques, temperature and process drift issues, test compaction and design validation, analog BIST, and functional test and verification issues. Also covered are STIL extension, IDDQ test, and on-line testing and fault tolerance. Lacks a subject index. Annotation copyrighted by Book News, Inc., Portland, OR.

2000 HD International Conference on High-Density Interconnect and Systems Packaging

19th IEEE VLSI Test Symposium

Proceedings of the 11th Asian Test Symposium : 18-20 November, 2002, Guam, USA

Advanced Packaging

Proceedings : 30 April-4 May 2000, Montréal, Québec, Canada

Wafer-Level Testing and Test During Burn-In for Integrated Circuits

Proceedings of the Technical Conference