Cmos Vlsi Design Weste Solution Manual

Designers of high-speed integrated circuits face a bewildering array of choices and too often spend frustrating days tweaking gates to meet speed targets. Logical Effort: Designing Fast CMOS Circuits makes high speed design easier and more methodical, providing a simple and broadly applicable method for estimating the delay resulting from factors such as topology, capacitance, and gate sizes. The brainchild of circuit and computer graphics pioneers Ivan Sutherland and Bob Sproull, "logical effort" will change the way you approach design challenges. This book begins by equipping you with a sound understanding of the method's essential procedures and concepts-so you can start using it immediately. Later chapters explore the theory and finer points of the method and detail its specialized applications. Features Explains the method and how to apply it in two practically focused chapters. Improves circuit design intuition by teaching simple ways to discern the consequences of topology and gate size decisions. Offers easy ways to choose the fastest circuit from among an array of potential circuit designs. Reduces the time spent on tweaking and simulations-so you can rapidly settle on a good design. Offers in-depth coverage of specialized areas of application for logical effort: skewed or unbalanced gates, other circuit families (including pseudo-NMOS and domino), wide structures such as decoders, and irregularly forking circuits. Presents a complete derivation of the method-so you see how and why it works.

This volume contains the proceedings from the workshops held in conjunction with the IEEE International Parallel and Distributed Processing Symposium, IPDPS 2000, on 1-5 May 2000 in Cancun, Mexico. The workshopsprovidea forum for bringing together researchers,practiti- ers, and designers from various backgrounds to discuss the state of the art in parallelism.Theyfocusondi erentaspectsofparallelism,fromruntimesystems to formal methods, from optics to irregular problems, from biology to networks of personal computers, from embedded systems to programming environments; the following workshops are represented in this volume: { Workshop on Personal Computer Based Networks of Workstations { Workshop on Advances in Parallel and Distributed Computational Models { Workshop on Par. and Dist. Comp. in Image, Video, and Multimedia { Workshop on High-Level Parallel Prog. Models and Supportive Env. { Workshop on High Performance Data Mining { Workshop on Solving Irregularly Structured Problems in Parallel { Workshop on Java for Parallel and Distributed Computing { WorkshoponBiologicallyInspiredSolutionsto ParallelProcessingProblems { Workshop on Parallel and Distributed Real-Time Systems { Workshop on Embedded HPC Systems and Applications { Recon gurable Architectures Workshop { Workshop on Formal Methods for Parallel Programming { Workshop on Optics and Computer Science { Workshop on Run-Time Systems for Parallel Programming { Workshop on Fault-Tolerant Parallel and Distributed Systems All papers published in the workshops proceedings were selected by the p- gram committee on the basis of referee reports. Each paper was reviewed by

independent referees who judged the papers for originality, quality, and cons- tency with the themes of the workshops.

CD-ROM contains: AIM SPICE (from AIM Software) -- Micro-Cap 6 (from Spectrum Software) -- Silos III Verilog Simulator (from Simucad) -- Adobe Acrobat Reader 4.0 (from Adobe).

STEEL DESIGN covers the fundamentals of structural steel design with an emphasis on the design of members and their connections, rather than the integrated design of buildings. The book is designed so that instructors can easily teach LRFD, ASD, or both, time-permitting. The application of fundamental principles is encouraged for design procedures as well as for practical design, but a theoretical approach is also provided to enhance student development. While the book is intended for junior-and senior-level engineering students, some of the later chapters can be used in graduate courses and practicing engineers will find this text to be an essential reference tool for reviewing current practices. Important Notice: Media content referenced within the product description or the product text may not be available in the ebook version.

A Systems Perspective with Verilog/VHDL Manual

IC Interconnect Analysis

Intelligent System Solutions for Auto Mobility and Beyond

Parallel and Distributed Processing

CMOS VLSI Design: A Circuits and Systems Perspective

CMOS VLSI Design: A Circuits and Systems PerspectivePearson Education IndiaVLSI DesignBoD – Books on Demand

Introduction The exponential scaling of feature sizes in semiconductor technologies has side-effects on layout optimization, related to effects such as inter connect delay, noise and crosstalk, signal integrity, parasitics effects, and power dissipation, that invalidate the assumptions that form the basis of previous design methodologies and tools. This book is intended to sample the most important, contemporary, and advanced layout opti mization problems emerging with the advent of very deep submicron technologies in semiconductor processing. We hope that it will stimulate more people to perform research that leads to advances in the design and development of more efficient, effective, and elegant algorithms and design tools. Organization of the Book The book is organized as follows. A multi-stage simulated annealing algorithm that integrates floorplanning and interconnect planning is pre sented in Chapter 1. To reduce the run time, different interconnect plan ning approaches are applied in different ranges of temperatures. Chapter 2 introduces a new design methodology - the interconnect-centric design methodology and its centerpiece, interconnect planning, which consists of physical hierarchy generation, floorplanning with interconnect planning, and interconnect architecture planning. Chapter 3 investigates a net-cut minimization based placement tool, Dragon, which integrates the state of the art partitioning and placement techniques.

Praise for CMOS: Circuit Design, Layout, and SimulationRevised Second Edition from the Technical Reviewers "A refreshing industrial flavor. Design concepts are presented as they are needed for 'just-in-time' learning. Simulating and designing circuits using SPICE is emphasized with literally hundreds of examples. Very few textbooks contain as much detail as this one. Highly recommended!" --Paul M. Furth, New Mexico State University "This book builds

a solid knowledge of CMOS circuit design from the ground up. With coverage of process integration, layout, analog and digital models, noise mechanisms, memory circuits, references, amplifiers, PLLs/DLLs, dynamic circuits, and data converters, the text is an excellent reference for both experienced and novice designers alike." --Tyler J. Gomm, Design Engineer, Micron Technology, Inc. "The Second Edition builds upon the success of the first with new chapters that cover additional material such as oversampled converters and non-volatile memories. This is becoming the de facto standard textbook to have on every analog and mixed-signal designer's bookshelf." --Joe Walsh, Design Engineer, AMI Semiconductor CMOS circuits from design to implementation CMOS: Circuit Design, Layout, and Simulation, Revised Second Edition covers the practical design of both analog and digital integrated circuits, offering a vital, contemporary view of a wide range of analog/digital circuit blocks, the BSIM model, data converter architectures, and much more. This edition takes a two-path approach to the topics: design techniques are developed for both long- and short-channel CMOS technologies and then compared. The results are multidimensional explanations that allow readers to gain deep insight into the design process. Features include: Updated materials to reflect CMOS technology's movement into nanometer sizes Discussions on phase- and delay-locked loops, mixed-signal circuits, data converters, and circuit noise More than 1,000 figures, 200 examples, and over 500 end-of-chapter problems In-depth coverage of both analog and digital circuit-level design techniques Real-world process parameters and design rules The book's Web site, CMOSedu.com, provides: solutions to the book's problems; additional homework problems without solutions; SPICE simulation examples using HSPICE, LTspice, and WinSpice; layout tools and examples for actually fabricating a chip; and videos to aid learning

Algorithms for VLSI Physical Design Automation is a core reference text for graduate students and CAD professionals. It provides a comprehensive treatment of the principles and algorithms of VLSI physical design. Algorithms for VLSI Physical Design Automation presents the concepts and algorithms in an intuitive manner. Each chapter contains 3-4 algorithms that are discussed in detail. Additional algorithms are presented in a somewhat shorter format. References to advanced algorithms are presented at the end of each chapter. Algorithms for VLSI Physical Design Automation covers all aspects of physical design. The first three chapters provide the background material while the subsequent chapters focus on each phase of the physical design cycle. In addition, newer topics like physical design automation of FPGAs and MCMs have been included. The author provides an extensive bibliography which is useful for finding advanced material on a topic. Algorithms for VLSI Physical Design Automation is an invaluable reference for professionals in layout, design automation and physical design.

Algorithms for VLSI Physical Design Automation

Logical Effort

CMOS VLSI Design

Practical Problems in VLSI Physical Design Automation

A Top-down Design Solution for Improved Testability in High Performance Circuits and Systems

Introduction to VLSI Circuits and Systems

System-on-a-Chip (SOC) integrated circuits composed of embedded cores are now commonplace. Nevertheless, there remain several roadblocks to rapid and efficient system integration. Test development is seen as a major bottleneck in SOC design and manufacturing capabilities. Testing SOCs is especially challenging in the absence of standardized test structures, test automation tools, and test protocols. In addition, long interconnects, high density, and high-speed designs lead to new types of faults

involving crosstalk and signal integrity. SOC (System-on-a-Chip) Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing. SOC (System-on-a-Chip) Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing.

This book provides a survey of the state of the art of technology and future trends in the new family of Smart Power ICs and describes design and applications in a variety of fields ranging from automotive to telecommunications, reliability evaluation and qualification procedures. The book is a valuable source of information and reference for both power IC design specialists and to all those concerned with applications, the development of digital circuits and with system architecture.

This book teaches basic and advanced concepts, new methodologies and recent developments in VLSI technology with a focus on low power design. It provides insight on how to use Tanner Spice, Cadence tools, Xilinx tools, VHDL programming and Synopsis to design simple and complex circuits using latest state-of-the art technologies. Emphasis is placed on fundamental transistor circuit-level design concepts.

Algorithms for VLSI Physical Design Automation, Second Edition is a core reference text for graduate students and CAD professionals. Based on the very successful First Edition, it provides a comprehensive treatment of the principles and algorithms of VLSI physical design, presenting the concepts and algorithms in an intuitive manner. Each chapter contains 3-4 algorithms that are discussed in detail. Additional algorithms are presented in a somewhat shorter format. References to advanced algorithms are presented at the end of each chapter. Algorithms for VLSI Physical Design Automation covers all aspects of physical design. In 1992, when the First Edition was published, the largest available microprocessor had one million transistors and was fabricated using three metal layers. Now we process with six metal layers, fabricating 15 million transistors on a chip. Designs are moving to the 500-700 MHz frequency goal. These stunning developments have significantly altered the VLSI field: over-the-cell routing and early floorplanning have come to occupy a central place in the physical design flow. This Second Edition introduces a realistic picture to the reader, exposing the concerns facing the VLSI industry, while maintaining the theoretical flavor of the First Edition. New material has been added to all chapters, new sections have been added to most chapters, and a few chapters have been completely rewritten. The textual material is supplemented and clarified by many helpful figures. Audience: An invaluable reference for professionals in layout, design automation and physical design.

Low Power VLSI Design
9th International Workshops, FPL'99, Glasgow, UK, August 30 - September 1, 1999, Proceedings
10th International Conference, FPL 2000 Villach, Austria, August 27-30, 2000 Proceedings
ALGORITHMS VLSI DESIGN AUTOMATION
Field-Programmable Logic and Applications. The Roadmap to Reconfigurable Computing
Wireless Security: Models, Threats, and Solutions

Practical Problems in VLSI Physical Design Automation contains problems and solutions related to various well-known algorithms used in VLSI physical design automation. Dr. Lim believes that the best way to learn new algorithms is to walk through a small example by hand. This knowledge will greatly help understand, analyze, and improve some of the well-known algorithms. The au has designed and taught a graduate-level course on physical CAD for VLSI at Georgia Tech. Over the years he has written his homework with such a focus and has maintained typeset version of the solutions.

BPP Learning Media is an ACCA Approved Content Provider. Our partnership with ACCA means that our Study Texts, Practice & Revision Kits and iPass (for CBE papers only) are subject to a thorough ACCA examining team review. Our suite of study tools w provide you with all the accurate and up-to-date material you need for exam success.

Low Power Design Methodologies presents the first in-depth coverage of all the layers of the design hierarchy, ranging from the technology, circuit, logic and architectural levels, up to the system layer. The book gives insight into the mechanisms of power dissipation in digital circuits and presents state of the art approaches to power reduction. Finally, it introduces a global view of low power design methodologies and how these are being captured in the latest design automation environments. The individual cha are written by the leading researchers in the area, drawn from both industry and academia. Extensive references are included at t end of each chapter. Audience: A broad introduction for anyone interested in low power design. Can also be used as a text book an advanced graduate class. A starting point for any aspiring researcher.

Books are seldom finished. At best, they are abandoned. The second edition of "Electronic Properties of Materials" has been in u now for about seven years. During this time my publisher gave me ample opportunities to update and improve the text whenever Ibook was reprinted. There were about six of these reprinting cycles. Eventually, however, it became clear that substantially more new material had to be added to account for the stormy developments which occurred in the field of electrical, optical, and magne materials. In particular, expanded sections on flat-panel displays (liquid crystals, electroluminescence devices, field emission displays, and plasma dis. : plays) were added. Further, the recent developments in blue- and green emitting LED's and in photoni are included. Magnetic storage devices also underwent rapid development. Thus, magneto-optical memories, magneto resistance devices, and new' magnetic materials needed to be covered. The sections on dielectric properties, ferroelectricity, piezoelectricity

electrostric tion, and thermoelectric properties have been expanded. Of course, the entire text was critically reviewed, updated, a improved. However, the most extensive change I undertook was the conversion of all equations to SI units throughout. In most of world and in virtually all of the interna tional scientific journals use of this system of units is required. If today's students do not lea to utilize it, another generation is "lost" on this matter. In other words, it is important that students become comfortable with SI uni

CMOS Digital Integrated Circuits

Design for Testability

Layout Optimization in VLSI Design

Theory of CMOS Digital Circuits and Circuit Failures

A Special Issue of Analog Integrated Circuits and Signal Processing, An International Journal Volume 14, Nos. 1/2 (1997)

Analysis and Design

Analog Design Issues in Digital VLSI Circuits and Systems brings together in one place important contributions and up-to-date research results in this fast moving area. Analog Design Issues in Digital VLSI Circuits and Systems serves as an excellent reference, providing insight into some of the most challenging research issues in the field.

CMOS chips are becoming increasingly important in computer circuitry. They have been widely used during the past decade, and they will continue to grow in popularity in those application areas that demand high performance. Challenging the prevailing opinion that circuit simulation can reveal all problems in CMOS circuits, Masakazu Shoji maintains that simulation cannot completely remove the often costly errors that occur in circuit design. To address the failure modes of these circuits more fully, he presents a new approach to CMOS circuit design based on his systematizing of circuit design error and his unique theory of CMOS digital circuit operation. In analyzing CMOS digital circuits, the author focuses not on effects originating from the characteristics of the device (MOSFET) but on those arising from their connection. This emphasis allows him to formulate a powerful but ultimately simple theory explaining the effects of connectivity by using a concept of the states of the circuits, called microstates. Shoji introduces microstate sequence diagrams that describe the state changes (or the circuit connectivity changes), and he uses his microstate theory to analyze many of the conventional CMOS digital circuits. These analyses are practically all in closed-form, and they provide easy physical interpretation of the circuit's working mechanisms, the parametric dependence of performance, and the circuit's failure modes. Originally published in 1992. The Princeton Legacy Library uses the latest print-on-demand technology to again make available previously out-of-print books from the distinguished backlist of Princeton University Press. These editions preserve the original texts of these important books while presenting them in durable paperback and hardcover editions. The goal of

the Princeton Legacy Library is to vastly increase access to the rich scholarly heritage found in the thousands of books published by Princeton University Press since its founding in 1905.

This book gathers papers from the 23rd International Forum on Advanced Microsystems for Automotive Applications (AMAA 2020) held online from Berlin, Germany, on May 26-27, 2020. Focusing on intelligent system solutions for auto mobility and beyond, it discusses in detail innovations and technologies enabling electrification, automation and diversification, as well as strategies for a better integration of vehicles into the networks of traffic, data and power. Further, the book addresses other relevant topics, including the role of human factors and safety issues in automated driving, solutions for shared mobility, as well as automated bus transport in rural areas. Implications of current circumstances, such as those generated by climate change, on the future development of auto mobility, are also analysed, providing researchers, practitioners and policy makers with an authoritative snapshot of the state-of-the-art, and a source of inspiration for future developments and collaborations.

This book conveys an understanding of CMOS technology, circuit design, layout, and system design sufficient to the designer. The book deals with the technology down to the layout level of detail, thereby providing a bridge from a circuit to a form that may be fabricated. The early chapters provide a circuit view of the CMOS IC design, the middle chapters cover a sub-system view of CMOS VLSI, and the final section illustrates these techniques using a real-world case study.

15 IPDPS 2000 Workshops Cancun, Mexico, May 1–5, 2000 Proceedings

Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs

Fundamentals

Advanced Microsystems for Automotive Applications 2020

Smart Power ICs

Electronic Properties of Materials

Modern microelectronic design is characterized by the integration of full systems on a single die. These systems often include large high performance digital circuitry, high resolution analog parts, high driving I/O, and maybe RF sections. Designers of such systems are constantly faced with the challenge to achieve compatibility in electrical characteristics of every section: some circuitry presents fast transients and large consumption spikes, whereas others require quiet environments to achieve resolutions well beyond millivolts. Coupling between those sections is usually unavoidable, since the entire system shares the same silicon substrate bulk and the same package. Understanding the way coupling is produced, and knowing methods to isolate coupled circuitry, and how to apply every method, is then mandatory knowledge for every IC designer. Analysis and Solutions for

Switching Noise Coupling in Mixed-Signal ICs is an in-depth look at coupling through the common silicon substrate, and noise at the power supply lines. It explains the elementary knowledge needed to understand these phenomena and presents a review of previous works and new research results. The aim is to provide an understanding of the reasons for these particular ways of coupling, review and suggest solutions to noise coupling, and provide criteria to apply noise reduction. Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs is an ideal book, both as introductory material to noise-coupling problems in mixed-signal ICs, and for more advanced designers facing this problem.

Aimed primarily for undergraduate students pursuing courses in VLSI design, the book emphasizes the physical understanding of underlying principles of the subject. It not only focuses on circuit design process obeying VLSI rules but also on technological aspects of Fabrication. VHDL modeling is discussed as the design engineer is expected to have good knowledge of it. Various Modeling issues of VLSI devices are focused which includes necessary device physics to the required level. With such an in-depth coverage and practical approach practising engineers can also use this as ready reference.

This is an up-to-date treatment of the analysis and design of CMOS integrated digital logic circuits. The self-contained book covers all of the important digital circuit design styles found in modern CMOS chips, emphasizing solving design problems using the various logic styles available in CMOS.

This book provides some recent advances in design nanometer VLSI chips. The selected topics try to present some open problems and challenges with important topics ranging from design tools, new post-silicon devices, GPU-based parallel computing, emerging 3D integration, and antenna design. The book consists of two parts, with chapters such as: VLSI design for multi-sensor smart systems on a chip, Three-dimensional integrated circuits design for thousand-core processors, Parallel symbolic analysis of large analog circuits on GPU platforms, Algorithms for CAD tools VLSI design, A multilevel memetic algorithm for large SAT-encoded problems, etc.

Low-Power VLSI Circuits and Systems

VLSI Design

ACCA F4 Corporate and Business Law (Global)

The Design and Analysis of VLSI Circuits

Analog Design Issues in Digital VLSI Circuits and Systems

Basic VLSI Design

The second edition of VLSI Design is a comprehensive textbook designed for undergraduate students of electrical, electronics, and electronics and communication engineering. It provides a thorough understanding of the fundamental concepts and design of VLSI systems.

This self-contained book addresses the need for analysis, characterization, estimation, and optimization of the various forms of power dissipation in the presence of process variations of nano-CMOS technologies. The authors show very large-scale integration (VLSI) researchers and engineers how to minimize the different types of power consumption of digital circuits. The material deals primarily with high-level (architectural or behavioral) energy dissipation.

This textbook provides a comprehensive, fully-updated introduction to the essentials of nanometer CMOS integrated circuits. It includes aspects of scaling to even beyond 12nm CMOS technologies and designs. It clearly describes the fundamental CMOS operating principles and presents substantial insight into the various aspects of design implementation and application. Coverage includes all associated disciplines of nanometer CMOS ICs, including physics, lithography, technology, design, memories, VLSI, power consumption, variability, reliability and signal integrity, testing, yield, failure analysis, packaging, scaling trends and road blocks. The text is based upon in-house Philips, NXP Semiconductors, Applied Materials, ASML, IMEC, ST-Ericsson, TSMC, etc., courseware, which, to date, has been completed by more than 4500 engineers working in a large variety of related disciplines: architecture, design, test, fabrication process, packaging, failure analysis and software.

For both introductory and advanced courses in VLSI design, this authoritative, comprehensive textbook is highly accessible to beginners, yet offers unparalleled breadth and depth for more experienced readers. The Fourth Edition of CMOS VLSI Design: A Circuits and Systems perspective presents broad and in-depth coverage of the entire field of modern CMOS VLSI Design. The authors draw upon extensive industry and classroom experience to introduce today's most advanced and effective chip design practices. They present extensively updated coverage of every key element of VLSI design, and illuminate the latest design challenges with 65 nm process examples. This book contains unsurpassed circuit-level coverage, as well as a rich set of problems and worked examples that provide deep practical insight to readers at all levels.

CMOS

Field Programmable Logic and Applications

Technologies and Applications

Steel Design

From Basics to ASICs

VLSI Test Principles and Architectures

The book provides a comprehensive coverage of different aspects of low power circuit synthesis at various levels of design hierarchy; starting from the layout level to the system level. For a seamless understanding of the subject, basics of MOS circuits has been introduced at transistor, gate and circuit level; followed by various low-power design methodologies, such as supply voltage scaling, switched capacitance minimization techniques and leakage power minimization approaches. The content of this book will prove useful to students, researchers, as well as practicing engineers.

Market_Desc: · Electrical Engineering Students taking courses on VLSI systems, CAD tools for VLSI, Design Automation at Final Year or Graduate Level, Computer Science courses on the same topics, at a similar level· Practicing Engineers wishing to learn the state of the art in VLSI Design Automation· Designers of CAD tools for chip design in software houses or large electronics companies. Special Features: · Probably the first book on Design Automation for VLSI Systems which covers all stages of design from layout synthesis through logic synthesis to high-level synthesis· Clear, precise presentation of examples, well illustrated with over 200 figures· Focus on algorithms for VLSI design tools means it will appeal to some Computer Science as well as Electrical Engineering departments About The Book: Enrollments in VLSI design automation courses are not large but it's a very popular elective, especially for those seeking a career in the microelectronics industry. Already the reviewers seem very enthusiastic about the coverage of the book being a better match for their courses than available competitors, because it covers all design phases. It has plenty of worked problems and a large no. of illustrations. It's a good 'list-builder' title that matches our strategy of focusing on topics that lie on the interface between Elec Eng and Computer Science.

This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product, drive down test cost, improve product quality and yield, and speed up time-to-market and time-to-volume. Most up-to-date coverage of design for testability. Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books. Numerous, practical examples in each chapter

illustrating basic VLSI test principles and DFT architectures.
The fourth edition of CMOS Digital Integrated Circuits: Analysis and Design continues the well-established tradition of the earlier editions by offering the most comprehensive coverage of digital CMOS circuit design, as well as addressing state-of-the-art technology issues highlighted by the widespread use of nanometer-scale CMOS technologies. In this latest edition, virtually all chapters have been re-written, the transistor model equations and device parameters have been revised to reflect the sigificant changes that must be taken into account for new technology generations, and the material has been reinforced with up-to-date examples. The broad-ranging coverage of this textbook starts with the fundamentals of CMOS process technology, and continues with MOS transistor models, basic CMOS gates, interconnect effects, dynamic circuits, memory circuits, arithmetic building blocks, clock and I/O circuits, low power design techniques, design for manufacturability and design for testability.
Nanometer CMOS ICs
??VLSI????
A Circuits and Systems Perspective
Principles and Applications
Designing Fast CMOS Circuits
Low-Power High-Level Synthesis for Nanoscale CMOS Circuits
This book constitues the refereed proceedings of the 10th International Conference on Field-Programmable Logic and Applications, FPL 2000, held in Villach, Austria in August 2000. The 64 revised full papers presented together with eight invited contributions and 21 short papers were carefully reviewed and selected from a total of 131 submissions. The book offers topical sections on network processors, prototyping, dynamic reconfigurability, technology mapping/routing and placement, biologically inspired methods, mobile communciation, design space exploration, optimization, architectures, methodology and technology, compilation, applications, and miscellaneous.
Nichols and Lekkas uncover the threats and vunerablilities unique to the wireless communication, telecom, broadband, and satellite markets. They provide an overview of

current commercial security solutions available on the open market.
As integrated circuit (IC) feature sizes scaled below a quarter of a micron, thereby defining the deep submicron (DSM) era, there began a gradual shift in the impact on performance due to the metal interconnections among the active circuit components. Once viewed as merely parasitics in terms of their relevance to the overall circuit behavior, the interconnect can now have a dominant impact on the IC area and performance. Beginning in the late 1980's there was significant research toward better modeling and characterization of the resistance, capacitance and ultimately the inductance of on-chip interconnect. IC Interconnect Analysis covers the state-of-the-art methods for modeling and analyzing IC interconnect based on the past fifteen years of research. This is done at a level suitable for most practitioners who work in the semiconductor and electronic design automation fields, but also includes significant depth for the research professionals who will ultimately extend this work into other areas and applications. IC Interconnect Analysis begins with an in-depth coverage of delay metrics, including the ubiquitous Elmore delay and its many variations. This is followed by an outline of moment matching methods, calculating moments efficiently, and Krylov subspace methods for model order reduction. The final two chapters describe how to interface these reduced-order models to circuit simulators and gate-level timing analyzers respectively. IC Interconnect Analysis is written for CAD tool developers, IC designers and graduate students.
This book contains the papers presented at the 9th International Workshop on Field ProgrammableLogic and Applications (FPL'99), hosted by the University of Strathclyde in Glasgow, Scotland, August 30 - September 1, 1999. FPL'99 is the ninth in the series of annual FPL workshops. The FPL'99 programme committee has been fortunate to have received a large number of high-quality papers addressing a wide range of topics. From these, 33 papers have been selected for presentation at the workshop and a further 32 papers have been accepted for the poster sessions. A total of 65 papers from 20 countries are included in this volume. FPL is a subject area that attracts researchers from both electronic engine- ing and computer science. Whether we are engaged in research into soft

ha- ware or hard software seems to be primarily a question of perspective. What is unquestionable is that the interaction of groups of researchers from di?erent backgrounds results in stimulating and productive research. As we prepare for the new millennium, the premier European forum for - searchers in ?eld programmable logic remains the FPL workshop. Next year the FPL series of workshopswill celebrate its tenth anniversary.The contribution of so many overseas researchers has been a particularly attractive feature of these events, giving them a truly international perspective, while the informal and convivial atmosphere that pervades the workshops have been their hallmark. We look forward to preserving these features in the future while continuing to expand the size and quality of the events.

Principles of CMOS VLSI Design

Circuit Design, Layout, and Simulation

SOC (System-on-a-Chip) Testing for Plug and Play Test Automation

CMOS Logic Circuit Design

Low Power Design Methodologies