Digital Circuit Testing And Testability

Device testing represents the single largest manufacturing expense in the semiconductor industry, costing over $40 billion a year. The most comprehensive and wide ranging book of its kind, Testing of Digital Systems covers everything you need to know about this vitally important subject. Starting right from the basics, the authors take the reader through automatic test pattern generation, design for testability and built-in self-test of digital circuits before moving on to more advanced topics such as IDDQ testing, functional testing, delay fault testing, memory testing, and fault diagnosis. The book includes detailed treatment of the latest techniques including test generation for various fault models, discussion of testing techniques at different levels of integrated circuit hierarchy and a chapter on system-on-a-chip test synthesis. Written for students and engineers, it is both an excellent senior/graduate level textbook and a valuable reference.

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In today’s digital design environment, engineers must achieve quick turn-around time with ready accesses to circuit synthesis and simulation applications. This type of productivity relies on the principles and practices of computer aided design (CAD). Digital Design: Basic Concepts and Principles addresses the many challenging issues critical to today’s digital design practices such as hazards and logic minimization, finite-state-machine synthesis, cycles and races, and testability theories while providing hands-on experience using one of the industry’s most popular design application, Xilinx Web PACKTM. The authors begin by discussing conventional and unconventional number systems, binary coding theories, and arithmetic as well as logic functions and Boolean algebra. Building upon classic theories of digital systems, the book illustrates the importance of logic minimization using the Karnaugh map technique. It continues by discussing implementation options and examining the pros and cons of each method in addition to an assessment of tradeoffs that often accompany design practices. The book also covers testability, emphasizing that a good digital design must be easy to verify and test with the lowest cost possible. Throughout the text, the authors analyze combinational and sequential logic elements and illustrate the designs of these components in structural, hierarchical, and behavior VHDL descriptions. Coveringfundamentals and best practices, Digital Design: Basic Concepts and Principles provides you with critical knowledge of how each digital component ties together to form a system and develops the skills you need to design and simulate these digital components using modern CAD software.

This book facilitates the VLSI-interested individuals with not only in-depth knowledge, but also the broad aspects of it by explaining its applications in different fields, including image processing and biomedical. The deep understanding of basic concepts gives you the power to develop a new application aspect, which is very well taken care of in this book by using simple language in explaining the concepts. In the VLSI world, the importance of hardware description languages cannot be ignored, as the designing of such dense and complex circuits is not possible without them. Both Verilog and VHDL languages are used here for designing. The current needs of high-performance integrated circuits (ICs) including low power devices and new emerging materials, which can play a very important role in achieving new functionalities, are the most interesting part of the book. The testing of VLSI circuits becomes more crucial than the designing of the circuits in this nanometer technology era. The role of fault simulation algorithms is very well explained, and its implementation using Verilog is the key aspect of this book. This book is well organized into 20 chapters. Chapter 1 emphasizes on uses of FPGA on various image processing and biomedical applications. Then, the descriptions enlighten the basic understanding of digital design from the perspective of HDL in Chapters 2–5. The performance enhancement with alternate material or geometry for silicon-based FET designs is focused in Chapters 6 and 7. Chapters 8 and 9 describe the study of bimolecular interactions with biosensing FETs. Chapters 10–13 deal with advanced FET structures available in various shapes, materials such as nanowire, HFET, and their comparison in terms of device performance metrics calculation. Chapters 14–18 describe different application-specific VLSI design techniques and challenges for analog and digital circuit designs. Chapter 19 explains the VLSI testability issues with the description of simulation and its categorization into logic and fault simulation for test pattern generation using Verilog HDL. Chapter 20 deals with a secured VLSI design with hardware obfuscation by hiding the IC’s structure and function, which makes it much more difficult to reverse engineer.

Next Generation Measures Using Formal Techniques
Testing and Reliable Design of CMOS Circuits
Testing and Diagnosis of Analog Circuits and Systems
Digital Logic Design
Digital Design

This book introduces several novel approaches to pave the way for the next generation of integrated circuits, which can be successfully and reliably integrated, even in safety-critical applications. The authors describe new measures to address the rising challenges in the field of design for testability, debug, and reliability, as strictly required for state-of-the-art circuit designs. In particular, this book combines formal techniques, such as the Satisfiability (SAT) problem and the Bounded Model Checking (BMC), to address the arising challenges concerning the increase in test data volume, as well as test application time and the required reliability. All methods are discussed in detail and evaluated extensively, while considering industry-relevant benchmark candidates. All measures have been integrated into a common framework, which implements standardized software/hardware interfaces.

This book is a self-contained introduction to all aspects of microelectronic (IC) testing. It includes the theory necessary for advanced students as well as reference to industrial practice and economics that will interest designers in industry. Chapters cover both digital circuit testing and the growing area of mixed circuits, used particularly in signal processing.

Power supply current monitoring to detect CMOS IC defects during production testing quietly laid down its roots in the mid-1970s. Both Sandia Labs and RCA in the United States and Philips Labs in the Netherlands practiced this procedure on their CMOS ICs. At that time, this practice stemmed simply from an intuitive sense that CMOS ICs showing abnormal quiescent power supply current (IDDQ) contained defects. Later, this intuition was supported by data and analysis in the 1980s by Levi (RACD, Malaiya and Su (SUNY-Binghamton), Soden and Hawkins (Sandia Labs and the University of New Mexico), Jacomino and co-workers (Laboratoire d'Automatique de Grenoble), and Maly and co-workers (Carnegie Mellon University). Interest in IDDQ testing has advanced beyond the data reported in the 1980s and is now focused on applications and evaluations involving larger volumes of ICs that improve quality beyond what can be achieved by previous conventional means. In the conventional style of testing one attempts to propagate the logic states of the suspended nodes to primary outputs. This is done for all or most nodes of the circuit. For sequential circuits, in particular, the complexity of finding suitable tests is very high. In comparison, the IDDQ test does not observe the logic states, but measures the integrated current that leaks through all gates. In other words, it is like measuring a patient's temperature to determine the state of health. Despite perceived advantages, during the years that followed its initial announcements, skepticism about the practicality of IDDQ testing prevailed. The idea, however, provided a great opportunity to researchers. New results on test generation, fault simulation, design for testability, built-in self-test, and diagnosis for this style of testing have since been reported. After a decade of research, we are definitely closer to practice.

This book is about digital system testing and testable design. The concepts of testing and testability are treated together with digital design practices and methodologies. The book uses Verilog models and testbenches for implementing and explaining fault simulation and test generation algorithms. Extensive use of Verilog and Verilog PLI for test applications is what distinguishes this book from other test and testability books. Verilog eliminates ambiguities in test algorithms and BIST and DFT hardware architectures, and it clearly describes the architecture of the testability hardware and its test sessions. Describing many of the on-chip decompression algorithms in Verilog helps to evaluate these algorithms in terms of hardware overhead and timing, and thus feasibility of using them for System-on-Chip designs. Extensive use of testbenches and testbench development techniques is another unique feature of this book. Using PLI in developing testbenches and virtual testers provides a powerful programming tool, interfaced with hardware described in Verilog. This mixed hardware/software environment facilitates description of complex test programs and test strategies.

Digital Circuit Testing and Testability
Digital Logic Circuit Analysis and Design (second Edition)
Logic Testing and Design for Testability
An Introduction
Design-for-Test Using Simulink and Stateflow

In the last few years CMOS technology has become increas ingly dominant for realizing Very Large Scale Integrated (VLSI) circuits. The popularity of this technology is due to its high den sity and low power requirement. The ability to realize very com plex circuits on a single chip has brought about a revolution in the world of electronics and computers. However, the rapid advance ments in this area pose many new problems in the area of testing. Testing has become a very time-consuming process. In order to ease the burden of testing, many schemes for designing the circuit for improved testability have been presented. These design for testability techniques have begun to catch the attention of chip manufacturers. The trend is towards placing increased emphasis on these techniques. Another byproduct of the increase in the complexity of chips is their higher susceptibility to faults. In order to take care of this problem, we need to build fault-tolerant systems. The area of fault-tolerant computing has steadily gained in importance. Today many universities offer courses in the areas of digital system testing and fault-tolerant computing. Due to the impor tance of CMOS technology, a significant portion of these courses may be devoted to CMOS testing. This book has been written as a reference text for such courses offered at the senior or graduate level. Familiarity with logic design and switching theory is assumed. The book should also prove to be useful to professionals working in the semiconductor industry.

The continual explosion of computer development has led to inadequate coverage of proper & useful on-line testing techniques. This text fills the gap in the literature by presenting the latest techniques available for digital devices used in the most popular computers. Initial chapters explore the classic problems of on-line testing, pointing out the limited applications of conventional approaches to the problem of diagnosing digital devices using LSI & VLSI chips. Chapters 4–7 cover compact testing methods used to diagnose complex digital circuits. Chapters 8 & 9 analyze the techniques of compressing output responses of a digital circuit, while chapter 10 surveys promising recent signature generation techniques for binary sequences. The final chapter covers multi-output digital circuits.

New, updated and expanded topics in the fourth edition include: EBCDIC, Grey code, practical applications of flip-flops, linear and shaft encoders, memory elements and FPGAs. The section on fault-finding has been expanded. A new chapter is dedicated to the interface between digital components and analog voltages. *A highly accessible, comprehensive and fully up to date digital systems text *A well known and respected text now revamped for current courses *Part of the Newnes suite of texts for HND/1st year modules

A current trend in digital design-the integration of the MATLAB® components Simulink® and Stateflow® for model building, simulations, system testing, and fault detection-allows for better control over the design flow process and, ultimately, for better system results. Digital Integrated Circuits: Design-for-Test Using Simulink® and Stateflow® illustrates the construction of Simulink models for digital project test benches in certain design-for-test fields. The first two chapters of the book describe the major tools used for design-for-test. The author explains the process of Simulink model building, presents the main library blocks of Simulink, and examines the development of finite-state machine modeling using Stateflow diagrams. Subsequent chapters provide examples of Simulink modeling and simulation for the latest design-for-test fields, including combinational and sequential circuits, controllability, and observability; deterministic algorithms; digital circuit dynamics; timing verification; built-in self-test (BIST) architecture; scan cell operations; and functional and diagnostic testing. The book also discusses the automatic test pattern generation (ATPG) process, the logical determinant theory, and joint test action group (JTAG) interface models. Digital Integrated Circuits explores the possibilities of MATLAB's tools in the development of application-specific integrated circuit (ASIC) design systems. The book shows how to incorporate Simulink and Stateflow into the process of modern digital design.

An Introduction to Logic Circuit Testing
Basic Concepts and Principles
Digital Circuit Testing
Using HDL Models and Architectures
Digital Integrated Circuits

Test and Design-for-Testability in Mixed-Signal Integrated Circuits deals with test and design for test of analog and mixed-signal integrated circuits. Especially in System-on-Chip (SoC), where different technologies are intertwined (analog, digital, sensors, RF), test is becoming a true bottleneck of present and future IC projects. Linking design and test in these heterogeneous systems will have a tremendous impact in terms of test time, cost and proficiency. Although it is recognized as a key issue for developing complex ICs, there is still a lack of structured references presenting the major topics in this area. The aim of this book is to present basic concepts and new ideas in a manner understandable for both professionals and students. Since this is an active research field, a comprehensive state-of-the-art overview is very valuable, introducing the main problems as well as the ways of solution that seem promising, emphasizing their basis, strengths and weaknesses. In essence, several topics are presented in detail. First of all, techniques for the efficient use of DSP-based test and CAD test tools. Standardization is another topic considered in the book, with focus on the IEEE 1149.4. Also addressed in depth is the connecting design and test by means of using high-level (behavioural) description techniques, specific examples are given. Another issue is related to test techniques for well-defined classes of integrated blocks, like data converters and phase-locked-loops. Besides these specification-driven testing techniques, fault-driven approaches are described as they offer potential solutions which are more similar to digital test methods. Finally, in Design-for-Testability and Built-In-Self-Test, two other concepts that were taken from digital design, are introduced in an analog context and illustrated for the case of integrated filters. In summary, the purpose of this book is to provide a glimpse on recent research results in the area of testing mixed-signal integrated circuits, specifically in the topics mentioned above. Much of the work reported herein has been performed within cooperative European Research Projects, in which the authors of the different chapters have actively collaborated. It is a representative snapshot of the current state-of-the-art in this emergent field.

This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product, drive down test cost, improve product quality and yield, and speed up time-to-market and time-to-volume. Most up-to-date coverage of design for testability. Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books. Numerous, practical examples in each chapter illustrating basic VLSI test principles and DFT architectures.

This updated printing of the leading text and reference in digital systems testing and testable design provides comprehensive, state-of-the-art coverage of the field. Included are extensive discussions of test generation, fault modeling for classic and new technologies, simulation, fault simulation, design for testability, built-in self-test, and diagnosis. Complete with numerous problems, this book is a must-have for test engineers, ASIC and system designers, and CAD developers, and advanced engineering students will find this book an invaluable tool to keep current with recent changes in the field.

"Introduces a theory of random testing in digital circuits for the first time and offers practical guidance for the implementation of random pattern generators, signature analyzers design for random testability, and testing results. Contains several new and unpublished results. "

Random Testing of Digital Circuits
Test and Design-for-Testability in Mixed-Signal Integrated Circuits
System-on-Chip Test Architectures
Nanometer Design for Testability
Design for Testability, Debug and Reliability

The summer school on VLSI GAD Tools and Applications was held from July 21 through August 1, 1986 at Beatenberg in the beautiful Bernese Oberland in Switzerland. The meeting was given under the auspices of IFIP WG 10. 6 VLSI, and it was sponsored by the Swiss Federal Institute of Technology Zurich, Switzerland. Eighty-one professionals were invited to participate in the summer school, including 18 lecturers. The 81 participants came from the following countries: Australia (1), Denmark (1), Federal Republic of Germany (12), France (3), Italy (4), Norway (1), South Korea (1), Sweden (5), United Kingdom (1), United States of America (13), and Switzerland (39). Our goal in the planning for the summer school was to introduce the audience into the realities of CAD tools and their applications to VLSI design. This book contains articles by all 18 invited speakers that lectured at the summer school. The reader should realize that it was not intended to publish a textbook. However, the chapters in this book are more or less self-contained treatments of the particular subjects. Chapters 1 and 2 give a broad introduction to VLSI Design. Simulation tools and their algorithmic foundations are treated in Chapters 3 to 5 and 17. Chapters 6 to 9 provide an excellent treatment of modern layout tools. The use of CAD tools and trends in the design of 32-bit microprocessors are the topics of Chapters 10 through 16. Important aspects in VLSI testing and testing strategies are given in Chapters 18 and 19.

IS THE TOPIC ANALOG TESTING AND DIAGNOSIS TIMELY? Yes, indeed it is. Testing and Diagnosis is an important topic and fulfills a vital need for the electronic industry. The testing and diagnosis of digital electronic circuits has been successfully developed to the point that it can be automated. Unfortu nately, its development for analog electronic circuits is still in its Stone Age. The engineer's intuition is still the most powerful tool used in the industry! There are two reasons for this. One is that there has been no pressing need from the industry. Analog circuits are usually small in size. Sometimes, the engineer's experience and intuition are sufficient to fulfill the need. The other reason is that there are no breakthrough results from academic re search to provide the industry with critical ideas to develop tools. This is not because of a lack of effort. Both academic and industrial research groups have made major efforts to look into this problem. Unfortunately, the prob lem for analog circuits is fundamentally different from and much more diffi cult than its counterpart for digital circuits. These efforts have led to some important findings, but are still not at the point of being practically useful. However, these situations are now changing. The current trend for the design of VLSI chips is to use analog/digital hybrid circuits, instead of digital circuits from the past. Therefore, even Ix x Preface though the analog circuit may be small, the total circuit under testing is large.

Using the book and the software provided with it, the reader can build his/her own tester arrangement to investigate key aspects of analog-, digital- and mixed system circuits Plan of attack based on traditional testing, circuit design and circuit manufacture allows the reader to appreciate a testing regime from the point of view of all the participating interests Worked examples based on theoretical bookwork, practical experimentation and simulation exercises teach the reader how to test circuits thoroughly and effectively

Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased performance-capacity demands from consumers. As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost. This book is a comprehensive guide to new VLSI Testing and Design-for-Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master quickly System-on-Chip Test architectures, for test debug and diagnosis of digital, memory, and analog/mixed-signal designs. Emphasizes VLSI Test principles and Design for Testability architectures, with numerous illustrations/examples. Most up-to-date coverage available, including Fault Tolerance, Low-Power Testing, Defect and Error Tolerance, Network-on-Chip (NOC) Testing, Software-Based Self-Testing, FPGA Testing, MEMS Testing, and System-In-Package (SIP) Testing, which are not yet available in any testing book. Covers the entire spectrum of VLSI testing and DFT architectures, from digital and analog, to memory circuits, and fault diagnosis and self-repair from digital to memory circuits. Discusses future nanotechnology test trends and challenges facing the nanometer design era; promising nanotechnology test techniques, including Quantum-Dots, Cellular Automata, Carbon-Nanotubes, and Hybrid Semiconductor/Nanowire/Molecular Computing. Practical problems at the end of each chapter for students.

A Guide to DFT and Other Techniques
A Designer's Guide to Built-In Self-Test
VLSI Testing
Testing Digital Circuits
Digital Logic Testing and Simulation

For sophomore courses on digital design in an Electrical Engineering, Computer Engineering, or Computer Science department. & Digital Design, fourth edition is a modern update of the classic authoritative text on digital design.& This book teaches the basic concepts of digital design in a clear, accessible manner. The book presents the basic tools for the design of digital circuits and provides procedures suitable for a variety of digital applications.

Recent technological advances have created a testing crisis in the electronics industry--smaller, more highly integrated electronic circuits and new packaging techniques make it increasingly difficult to physically access test nodes. New testing methods are needed for the next generation of electronic equipment and a great deal of emphasis is being placed on the development of these methods. Some of the techniques now becoming popular include design for testability (DFT), built-in self-test (BIST), and automatic test vector generation (ATVG). This book will provide a practical introduction to these and other testing techniques. For each technique introduced, the author provides real-world examples so the reader can achieve a working knowledge of how to choose and apply these increasingly important testing methods.

For those with a basic understanding of digital design, this book teaches the essential skills to design digital integrated circuits using Verilog and the relevant extensions of SystemVerilog. In addition to covering the syntax of Verilog and SystemVerilog, the author provides an appreciation of design challenges and solutions for producing working circuits. The book covers not only the syntax and limitations of HDL coding, but deals extensively with design problems such as partitioning and synchronization, helping you to produce designs that are not only logically correct, but will actually work when turned into physical circuits. Throughout the book, many small examples are used to validate concepts and demonstrate how to apply design skills. This book takes readers who have already learned the fundamentals of digital design to the point where they can produce working circuits using modern design methodologies. It clearly explains what is useful for circuit design and what parts of the languages are only software, providing a non-theoretical, practical guide to robust, reliable and optimized hardware design and development. Produce working hardware: Covers not only syntax, but also provides design know-how, addressing problems such as synchronization and partitioning to produce working solutions Usable examples: Numerous small examples throughout the book demonstrate concepts in an easy-to-grasp manner Essential knowledge: Covers the vital design topics of synchronization, essential for producing working silicon; asynchronous interfacing techniques; and design techniques for circuit optimization, including partitioning

Your road map for meeting today's digital testing challenges Today, digital logic devices are common in products that impact public safety, including applications in transportation and human implants. Accurate testing has become more critical to reliability, safety, and the bottom line. Yet, as digital systems become more ubiquitous and complex, the challenge of testing them has become more difficult. As one development group designing a RISC stated, "the work required to . . . test a chip of this size approached the amount of effort required to design it." A valued reference for nearly two decades, Digital Logic Testing and Simulation has been significantly revised and updated for designers and test engineers who must meet this challenge. There is no single solution to the testing problem. Organized in an easy-to-follow, sequential format, this Second Edition familiarizes the reader with the many different strategies for testing and their applications, and assesses the strengths and weaknesses of the various approaches. The book reviews the building blocks of a successful testing strategy and guides the reader on choosing the best solution for a particular application. Digital Logic Testing and Simulation, Second Edition covers such key topics as: * Binary Decision Diagrams (BDDs) and cycle-based simulation * Tester architectures/Standard Test Interface Language (STIL) * Practical algorithms written in a Hardware Design Language (HDL) * Fault tolerance * Behavioral Automatic Test Pattern Generation (ATPG) * The development of the Test Design Expert (TDX), the many obstacles encountered and lessons learned in creating this novel testing approach Up-to-date and comprehensive, Digital Logic Testing and Simulation is an important resource for anyone charged with pinpointing faulty products and assuring quality, safety, and profitability.

Design for Testability
Logic Design Principles
Modern Techniques
Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits
Advanced VLSI Design and Testability Issues

The modern electronic testing has a forty year history. Test professionals hold some fairly large conferences and numerous workshops, have a journal, and there are over one hundred books on testing. Still, a full course on testing is offered only at a few universities, mostly by professors who have a research interest in this area. Apparently, most professors would not have taken a course on electronic testing when they were students. Other than the computer engineering curriculum being too crowded, the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook. For VLSI the foundation was provided by semiconductor device techn- ogy, circuit design, and electronic testing. In a computer engineering curriculum, therefore, it is necessary that foundations should be taught before applications. The field of VLSI has expanded to systems-on-a-chip, which include digital, memory, and mixed-signalsubsystems. To our knowledge this is the first textbook to cover all three types of electronic circuits. We have written this textbook for an undergraduate “ foundations ” course on electronic testing. Obviously, it is too voluminous for a one-semester course and a teacher will have to select from the topics. We did not restrict such freedom because the selection may depend upon the individual expertise and interests. Besides, there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course. With equal tenacity, we address the needs of three other groups of readers.

In-Circuit Testing discusses what an in-circuit test (ICT) is and what it can and cannot do. It answers many questions on how tests are actually carried out, with the benefits and drawbacks of the techniques. The emphasis throughout is towards practical problem solving, and many of the examples used are of surface mount printed circuit boards (PCBs). The book contains separate chapters on application—fitting ICT into a typical test strategy and into the manufacturing environment. The buying decision is fully explored—choice of system, initial and ongoing costs, and preparation of the financial proposal to Management. Then, assuming the automatic test equipment (ATE) has been purchased, additional chapters are devoted to: programming problems and solutions, interfacing problems and solutions, fault diagnosis and fault finding tools. Design for in-circuit test also merits a chapter. This covers specific design guides and the constraints which need to be placed on designers to ensure that ICT is cost effective. The concluding chapter reviews the purchase and use of the chosen ICT with the benefit of hindsight; it covers cost effectiveness; looks at alternative methods of testing, programming, and interfacing; and alternative ways of costing the testing service. This book is written for potential purchasers and users of in-circuit automatic testers who are attracted to the concept of ICT, but who may need help. This includes Test Engineering Managers who need guidance on which equipment to buy for a given application (and how to financially justify the purchase), and ATE Programmers, Test Engineers and Technicians who would welcome practical advice on how best to use the chosen ATE.

In the early days of digital design, we were concerned with the logical correctness of circuits. We knew that if we slowed down the clock signal sufficiently, the circuit would function correctly. With improvements in the semiconductor process technology, our expectations on speed have soared. A frequently asked question in the last decade has been how fast can the clock run. This puts significant demands on timing analysis and delay testing. Fueled by the above events, a tremendous growth has occurred in the research on delay testing. Recent work includes fault models, algorithms for test generation and fault simulation, and methods for design and synthesis for testability. The authors of this book, Angela Krstic and Tim Cheng, have personally contributed to this research. Now they do an even greater service to the profession by collecting the work of a large number of researchers. In addition to expounding such a great deal of information, they have delivered it with utmost clarity. To further the reader's understanding many key concepts are illustrated by simple examples. The basic ideas of delay testing have reached a level of maturity that makes them suitable for practice. In that sense, this book is the best x DELAY FAULT TESTING FOR VLSI CIRCUITS available guide for an engineer designing or testing VLSI systems. Tech niques for path delay testing and for use of slower test equipment to test high-speed circuits are of particular interest.

An Introduction to Logic Circuit Testing provides a detailed coverage of techniques for test generation and testable design of digital electronic circuits/systems. The material covered in the book should be sufficient for a course, or part of a course, in digital circuit testing for senior-level undergraduate and first-year graduate students in Electrical Engineering and Computer Science. The book will also be a valuable resource for engineers working in the industry. This book has four chapters. Chapter 1 deals with various types of faults that may occur in very large scale integration (VLSI)-based digital circuits. Chapter 2 introduces the major concepts of all test generation techniques such as redundancy, fault coverage, sensitization, and backtracking. Chapter 3 introduces the key concepts of testability, followed by some ad hoc design-for-testability rules that can be used to enhance testability of combinational circuits. Chapter 4 deals with test generation and response evaluation techniques used in BIST (built-in self-test) schemes for VLSI chips. Table of Contents: Introduction / Fault Detection in Logic Circuits / Design for Testability / Built-in Self-Test / References

VLSI CAD Tools and Applications
Delay Fault Testing for VLSI Circuits
Fault Diagnosis of Digital Circuits
Digital Systems Testing and Testable Design
Notes, Observations and Improvements in the Area of Digital Circuit Testing and Testability

Enables the reader to test an analog circuit that is implemented either in bipolar or MOS technology. Examines the testing and fault diagnosis of analog and analog part of mixed signal circuits. Covers the testing and fault diagnosis of both bipolar and Metal Oxide Semiconductor (MOS) circuits and introduces . Also contains problems that can be used as quiz or homework.

Today's computers must perform with increasing reliability, which in turn depends onthe problem of determining whether a circuit has been manufactured properly or behaves correctly.However, the greater circuit density of VLSI circuits and systems has made testing more difficultand costly. This book notes that one solution is to develop faster and more efficient algorithms togenerate test patterns or use design techniques to enhance testability - that is, "design fortestability." Design for testability techniques offer one approach toward alleviating this situationby adding enough extra circuitry to a circuit or chip to reduce the complexity of testing. Becausethe cost of hardware is decreasing as the cost of testing rises, there is now a growing interest inthese techniques for VLSI circuits.The first half of the book focuses on the problem of testing:test generation, fault simulation, and complexity of testing. The second half takes up the problemof design for testability: design techniques to minimize test application and/or test generationcost, scan design for sequential logic circuits, compact testing, built-in testing, and variousdesign techniques for testable systems.Hideo Fujiwara is an associate professor in the Department ofElectronics and Communication, Meiji University. Logic Testing and Design for Testability isincluded in the Computer Systems Series, edited by Herb Schwetman.

In the past few years, reliable hardware system design has become increasingly important in the computer industry. Digital Circuit Testing and Testability is an easy to use introduction to the practices and techniques in this field.Parag K. Lala writes in a user-friendly and tutorial style, making the book easy to read, even for the newcomer to fault-tolerant system design. Each informative chapter is self-contained, with little or no previous knowledge of a topic assumed. Extensive references follow each chapter, making further research in a particular area readily available. Each chapter covers a different aspect or technological component of fault-tolerant system design, and this book is an excellent compilation of up-to-date information in an area where such a book is needed.

A recent technological advance is the art of designing circuits to test themselves, referred to as a Built-In Self-Test. This book is written from a designer's perspective and describes the major BIST approaches that have been proposed and implemented, along with their advantages and limitations.

In–Circuit Testing
Theory and Applications
Design of Logic Systems
Integrated Circuit Test Engineering
Digital Integrated Circuit Design Using Verilog and Systemverilog