High Performance Asic Design Using Synthesizable Domino Logic In An Asic Flow

The recent evolution of digital technology has resulted in the design of digital processors with increasingly complex capabilities. The implementation of hardware/software co-design methodologies provides new opportunities for the development of low power, high speed DSPs and processor networks. Dedicated digital processors are digital processors with an application specific computational task. Dedicated Digital Processors presents an integrated and accessible approach to digital processor design principles, processes, and implementations based upon the author's considerable experience in teaching digital systems design and digital signal processing. Emphasis is placed on presentation of hardware/software co-design methods, with examples and illustrations provided throughout the text. System-on-a-chip and embedded systems are described and examples of high speed real-time processing are given. Coverage of standard and emerging DSP architectures enable the reader to make an informed selection when undertaking their own designs. Presents readers with the elementary building blocks for the design of digital hardware systems and processor networks Provides a unique evaluation of standard DSP architectures whilst providing up-to-date information on the latest architectures, including the TI 55x and TigerSharc chip families and the Virtex FPGA (field-programmable gate array) Introduces the concepts and methodologies for describing and designing hardware VHDL is presented and used to illustrate the design of a simple processor A practical overview of hardware/software codesign with design techniques and considerations illustrated with examples of real-world designs Fundamental reading for graduate and senior undergraduate students of computer and electronic engineering, and Practicing engineers developing DSP applications.

The chips in present-day cell phones already contain billions of sub-100-nanometer transistors. By 2020, however, we will see systems-on-chips with trillions of 10-nanometer transistors. But this will be the end of the miniaturization, because yet smaller transistors, containing just a few control atoms, are subject to statistical fluctuations and thus no longer useful. We also need to worry about a potential energy crisis, because in less than five years from now, with current chip technology, the internet alone would consume the total global electrical power! This book presents a new, sustainable roadmap towards ultra-low-energy (femto-Joule), high-performance electronics. The focus is on the energy-efficiency of the various chip functions: sensing, processing, and communication, in a top-down spirit involving new architectures such as silicon brains, ultra-low-voltage circuits, energy harvesting, and 3D silicon technologies. Recognized world leaders from industry and from the research community share their views of this nanoelectronics future. They discuss, among other things, ubiquitous communication based on mobile companions, health and care supported by autonomous implants and by personal carebots, safe and efficient mobility assisted by co-pilots equipped with intelligent micro-electromechanical systems, and internet-based education for a billion people from kindergarden to retirement. This book should help and interest all those who will have to make decisions associated with future electronics: students, graduates, educators, and researchers, as well as managers, investors, and policy makers. Introduction: Towards Sustainable 2020 Nanoelectronics.- From Microelectronics to Nanoelectronics.- The Future of Eight Chip Technologies.- Analog□Digital Interfaces.- Interconnects and Transceivers.- Requirements and Markets for Nanoelectronics.- ITRS: The International Technology Roadmap for Semiconductors.- Nanolithography.- Power-Efficient Design Challenges.- Superprocessors and Supercomputers.- Towards Terabit Memories.- 3D Integration for Wireless Multimedia.- The Next-Generation Mobile User-Experience.- MEMS (Micro-Electro-Mechanical Systems) for Automotive and Consumer.- Vision Sensors and Cameras.- Digital Neural Networks for New Media.- Retinal Implants for Blind Patients.- Silicon Brains.- Energy Harvesting and Chip Autonomy.- The Energy Crisis.- The Extreme-Technology Industry.- Education and Research for the Age of Nanoelectronics.- 2020 World with Chips.

From the Foreword..... Modern digital signal processing applications provide a large challenge to the system designer. Algorithms are becoming increasingly complex, and yet they must be realized with tight performance constraints. Nevertheless, these DSP algorithms are often built from many constituent canonical subtasks (e.g., IIR and FIR filters, FFTs) that can be reused in other subtasks. Design is then a problem of composing these core entities into a cohesive whole to provide both the intended functionality and the required performance. In order to organize the design process, there have been two major approaches. The top-down approach starts with an abstract, concise, functional description which can be quickly generated. On the other hand, the bottom-up approach starts from a detailed low-level design where performance can be directly assessed, but where the requisite design and interface detail take a long time to generate. In this book, the authors show a way to effectively resolve this tension by retaining the high-level conciseness of VHDL while parameterizing it to get good fit to specific applications through reuse of core library components. Since they build on a pre-designed set of core elements, accurate area, speed and power estimates can be percolated to high- level design routines which explore the design space. Results are impressive, and the cost model provided will prove to be very useful. Overall, the authors have provided an up-to-date approach, doing a good job at getting performance out of high-level design. The methodology provided makes good use of extant design tools, and is realistic in terms of the industrial design process. The approach is interesting in its own right, but is also of direct utility, and it will give the existing DSP CAD tools a highly competitive alternative. The techniques described have been developed within ARPAs RASSP (Rapid Prototyping of Application Specific Signal Processors) project, and should be of great interest there, as well as to many industrial designers. Professor Jonathan Allen, Massachusetts Institute of Technology

This book offers a compilation of technical papers presented at the International Research Symposium on Computing and Network Sustainability (IRSCNS 2018) held in Goa, India on 30□31st August 2018. It covers areas such as sustainable computing and security, sustainable systems and technologies, sustainable methodologies and applications, sustainable networks applications and solutions, user-centered services and systems and mobile data management. Presenting novel and recent technologies, it is a valuable resource for researchers and industry professionals alike.

16th International Symposium on VSLI Design and Test, VDAT 2012, Shipur, India, July 1-4, 2012, Proceedings

Tools and Techniques for Low Power Design

Computing and Network Sustainability

Energy Research Abstracts

Chips 2020

Closing the Power Gap between ASIC & Custom

Advanced HDL Synthesis and SOC Prototyping

This book describes best practices for successful FPGA design. It is the result of the author’s meetings with hundreds of customers on the challenges facing each of their FPGA design teams. By gaining an understanding into their design environments, processes, what works and what does not work, key areas of concern in implementing system designs have been identified and a recommended design methodology to overcome these challenges has been developed. This book’s

content has a strong focus on design teams that are spread across sites. The goal being to increase the productivity of FPGA design teams by establishing a common methodology across design teams; enabling the exchange of design blocks across teams. Coverage includes the complete FPGA design flow, from the basics to advanced techniques. This new edition has been enhanced to include new sections on System modeling, embedded design and high level design. The original sections on Design Environment, RTL design and timing closure have all been expanded to include more up to date techniques as well as providing more extensive scripts and RTL code that can be reused by readers. Presents complete, field-tested methodology for FPGA design, focused on reuse across design teams; Offers best practices for FPGA timing closure, in-system debug, and board design; Details techniques to resolve common pitfalls in designing with FPGAs.
This book constitutes the refereed proceedings of the 12th International Conference on High-Performance Computing, HiPC 2005, held in Goa, India in December 2005. The 50 revised full papers presented were carefully reviewed and selected from 362 submissions. After the keynote section and the presentation of the 2 awarded best contributions the papers are organized in topical sections on algorithms, applications, architecture, systems software, communication networks, and systems and networks.
This book describes digital design techniques with exercises. The concepts and exercises discussed are useful to design digital logic from a set of given specifications. Looking at current trends of miniaturization, the contents provide practical information on the issues in digital design and various design optimization and performance improvement techniques at logic level. The book explains how to design using digital logic elements and how to improve design performance. The book also covers data and control path design strategies, architecture design strategies, multiple clock domain design and exercises , low-power design strategies and solutions at the architecture and logic-design level. The book covers 60 exercises with solutions and will be useful to engineers during the architecture and logic design phase. The contents of this book prove useful to hardware engineers, logic design engineers, students, professionals and hobbyists looking to learn and use the digital design techniques during various phases of design.
This books focuses on recent break-throughs in the development of a variety of photonic devices, serving distances ranging from mm to many km, together with their electronic counter-parts, e.g. the drivers for lasers, the amplifiers following the detectors and most important, the relevant advanced VLSI circuits. It explains that as a consequence of the increasing dominance of optical interconnects for high performance workstation clusters and supercomputers their complete design has to be revised. This book thus covers for the first time the whole variety of interdependent subjects contributing to green photonics and electronics, serving communication and energy harvesting. Alternative approaches to generate electric power using organic photovoltaic solar cells, inexpensive and again energy efficient in production are summarized. In 2015, the use of the internet consumed 5-6% of the raw electricity production in developed countries. Power consumption increases rapidly and without some transformational change will use, by the middle of the next decade at the latest, the entire electricity production. This apocalyptic outlook led to a redirection of the focus of data center and HPC developers from just increasing bit rates and capacities to energy efficiency. The high speed interconnects are all based on photonic devices. These must and can be energy efficient but they operate in an electronic environment and therefore have to be considered in a wide scope that also requires low energy electronic devices, sophisticated circuit designs and clever architectures. The development of the next generation of high performance exaFLOP computers suffers from the same problem: Their energy consumption based on present device generations is essentially prohibitive.
Successful ASIC Design the First Time Through
Scientific and Technical Aerospace Reports
Core-Based Behavioral Synthesis
RTL Design Using Verilog
A Guide to the Future of Nanoelectronics
Vol 3, No 2: June 2014
FPGA Design

by Kurt Keutzer Those looking for a quick overview of the book should fast-forward to the Introduction in Chapter 1. What follows is a personal account of the creation of this book. The challenge from Earl Killian, formerly an architect of the MIPS processors and at that time Chief Architect at Tensilica, was to explain the significant performance gap between ASICs and custom circuits designed in the same process generation. The relevance of the challenge was amplified shortly thereafter by Andy Bechtolsheim, founder of Sun Microsystems and ubiquitous investor in the EDA industry. At a dinner talk at the 1999 International Symposium on Physical Design, Andy stated that the greatest near-term opportunity in CAD was to develop tools to bring the performance of ASIC circuits closer to that of custom designs. There seemed to be some synchronicity that two individuals so different in concern and character would be pre-occupied with the same problem. Intrigued by Earl and Andy's comments, the game was afoot. Earl Killian and other veterans of microprocessor design were helpful with clues as to the sources of the performance discrepancy: layout, circuit design, clocking methodology, and dynamic logic. I soon realized that I needed help in tracking down clues. Only at a wonderful institution like the University of California at Berkeley

could I so easily commandeer an ab- bodied graduate student like David Chinnery with a knowledge of architecture, circuits, computer-aided design and algorithms.

This book introduces the reader to FPGA based design for RTL synthesis. It describes simple to complex RTL design scenarios using SystemVerilog. The book builds the story from basic fundamentals of FPGA based designs to advance RTL design and verification concepts using SystemVerilog. It provides practical information on the issues in the RTL design and verification and how to overcome these. It focuses on writing efficient RTL codes using SystemVerilog, covers design for the Xilinx FPGAs and also includes implementable code examples. The contents of this book cover improvement of design performance, assertion based verification, verification planning, and architecture and system testing using FPGAs. The book can be used for classroom teaching or as a supplement in lab work for undergraduate and graduate coursework as well as for professional development and training programs. It will also be of interest to researchers and professionals interested in the RTL design for FPGA and ASIC.

This book describes RTL design, synthesis, and timing closure strategies for SOC blocks. It covers high-level RTL design scenarios and challenges for SOC design. The book gives practical information on the issues in SOC and ASIC prototyping using modern high-density FPGAs. The book covers SOC performance improvement techniques, testing, and system-level verification. The book also describes the modern Xilinx FPGA architecture and their use in SOC prototyping. The book covers the Synopsys DC, PT commands, and use of them to constraint and to optimize SOC design. The contents of this book will be of use to students, professionals, and hobbyists alike.

This book carefully details design tools and techniques for high-performance ASIC design. Using these techniques, the performance of ASIC designs can be improved by two to three times. Important topics include: Improving performance through microarchitecture; Timing-driven floorplanning; Controlling and exploiting clock skew; High performance latch-based design in an ASIC methodology; Automatically identifying and synthesizing complex logic gates; Automated cell sizing to increase performance and reduce power; Controlling process variation.These techniques are illustrated by designs running two to three times the speed of typical ASICs in the same process generation.

18th International Conference on Intelligent Systems Design and Applications (ISDA 2018) held in Vellore, India, December 6-8, 2018, Volume 1

Proceedings of IRSCNS 2018

A Practical Guide for FPGA and ASIC Implementations

Designing with High Performance ASICs

12th International Conference, Goa, India, December 18-21, 2005, Proceedings

Integrated Circuit and System Design: Power and Timing Modeling, Optimization and Simulation

Advances in Communication, Network, and Computing

Bulletin of Electrical Engineering and Informatics (Buletin Teknik Elektro dan Informatika) ISSN: 2089-3191, e-ISSN: 2302-9285 is open to submission from scholars and experts in the wide areas of electrical, electronics, instrumentation, control, telecommunication and computer engineering from the global world. The journal publishes original papers in the field of electrical, electronics, instrumentation & control, telecommunication, computer and informatics engineering. Vol 3, No 2 June 2014 Table of Contents Predictions on the Development Dimensions of Provincial Tourism Discipline Based on the Artificial Neural Network BP Model PDF Yang Yang, Jun Hu, Mu Zhang 69-76 Study on the Rough-set-based Clustering Algorithm for Sensor Networks PDF Fengmei Liang, Liyuan Zhang, Peng Sun 77-90 Varying Vector Pulse Width Modulation for Three Phase Inverter PDF Raju J, Kowsalya M 91-100 Optimal Determination of Size and Site of DGs in Mesh System Using PSO PDF Mohammad Salehi Male, Adel Akbari Majd, Ramtin Rasouli Nezhad 101-108 Voltage Sag Mitigation and Load Reactive Power Compensation by UPQC PDF P. Ajitha, D. Jananisri 109-112 A Power Quality Improvement for Microgrid Inverter Operated In Grid Connected and Grid Disconnected Modes PDF M. Tamil Selvi, D.G unapriya 113-118 Harmonic Reduction in Variable Frequency Drives Using Active Power Filter PDF M. Tamilvani, K. Nithya, M. Srinivasan, S.U Prabha 119-126 Sampled Reference Frame Algorithm Based on Space Vector Pulse Width Modulation for Five Level Cascaded H-Bridge Inverter PDF Gomathi C, Navya Nagath, Veerakumar S 127-140 Subthreshold Dual Mode Logic PDF J.Nageswara Reddy, T. Sathyanarayana, M.A. Khadar Baba 141-148

This book presents Dual Mode Logic (DML), a new design paradigm for digital integrated circuits. DML logic gates can operate in two modes, each optimized for a different metric. Its on-the-fly switching between these operational modes at the gate, block and system levels provide maximal E-D optimization flexibility. Each highly detailed chapter has multiple illustrations showing how the DML paradigm seamlessly implements digital circuits that dissipate less energy while simultaneously improving performance and reducing area without a significant compromise in reliability. All the facets of the DML methodology are covered, starting from basic concepts, through single gate optimization, general module optimization, design trade-offs and new ways DML can be integrated into standard design flows using standard EDA tools. DML logic is compatible with numerous applications but is particularly advantageous for ultra-low power, reliable high performance systems, and advanced scaled technologies Written in language accessible to students and design engineers, each topic is oriented toward immediate application by all those interested in an alternative to CMOS logic. Describes a novel, promising alternative to conventional CMOS logic, known as Dual Mode Logic (DML), with which a single gate can be operated selectively in two modes, each optimized for a different metric (e.g., energy consumption, performance, size); Demonstrates several techniques at the architectural level, which can result in high energy savings and improved system performance; Focuses on the tradeoffs between power, area and speed including optimizations at the transistor and gate level, including alternatives to DML basic cells; Illustrates DML efficiency for a variety of VLSI applications.

This second edition focuses on the thought process of digital design and implementation in the context of VLSI and system design. It covers the Verilog 2001 and Verilog 2005 RTL design styles, constructs and the optimization at the RTL and synthesis level. The book also covers the logic synthesis, low power, multiple clock domain design concepts and design performance improvement techniques. The book includes 250 design examples/illustrations and 100 exercise questions. This volume can be used as a core or supplementary text in undergraduate courses on logic design and as a text for professional and vocational coursework. In addition, it will be a hands-on professional reference and a self-study aid for hobbyists.

High Performance ASIC DesignUsing Synthesizable Domino Logic in an ASIC FlowCambridge University Press
Green Photonics and Electronics
Proceedings of ICCAN 2017
Using Synthesizable Domino Logic in an ASIC Flow
19th International Workshop, PATMOS 2009, Delft, The Netherlands, September 9-11, 2009, Revised Selected Papers
Logic Synthesis and SOC Prototyping
Progress in VLSI Design and Test
Bulletin of Electrical Engineering and Informatics

This book constitutes the thoroughly refereed post-conference proceedings of 19th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2009, featuring Integrated Circuit and System Design, held in Delft, The Netherlands during September 9-11, 2009. The 26 revised full papers and 10 revised poster papers presented were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on variability & statistical timing, circuit level techniques, power management, low power circuits & technology, system level techniques, power & timing optimization techniques, self-timed circuits, low power circuit analysis & optimization, and low power design studies.

This book is designed to serve as a hands-on professional reference with additional utility as a textbook for upper undergraduate and some graduate courses in digital logic design. This book is organized in such a way that that it can describe a number of RTL design scenarios, from simple to complex. The book constructs the logic design story from the fundamentals of logic design to advanced RTL design concepts. Keeping in view the importance of miniaturization today, the book gives practical information on the issues with ASIC RTL design and how to overcome these concerns. It clearly explains how to write an efficient RTL code and how to improve design performance. The book also describes advanced RTL design concepts such as low-power design, multiple clock-domain design, and SOC-based design. The practical orientation of the book makes it ideal for training programs for practicing design engineers and for short-term vocational programs. The contents of the book will also make it a useful read for students and hobbyists.

This book constitutes the thoroughly refereed proceedings of the Third International Conference on Advances in Communication, Network, and Computing, CNC 2012, held in Chennai, India, February 24-25, 2012. The 41 revised full papers presented together with 29 short papers and 14 poster papers were carefully selected and reviewed from 425 submissions. The papers cover a wide spectrum of issues in the field of Information Technology, Networks, Computational Engineering, Computer and Telecommunication Technology, ranging from theoretical and methodological issues to advanced applications.

This book constitutes the refereed proceedings of the 16th International Symposium on VSLI Design and Test, VDAT 2012, held in Shibpur, India, in July 2012. The 30 revised regular papers presented together with 10 short papers and 13 poster sessions were carefully selected from 135 submissions. The papers are organized in topical sections on VLSI design, design and modeling of digital circuits and systems, testing and verification, design for testability, testing memories and regular logic arrays, embedded systems: hardware/software co-design and verification, emerging technology: nanoscale computing and nanotechnology.

A Practice Book for Digital Logic Design
Best Practices for Team-based Reuse
Signal Integrity Effects in Custom IC and ASIC Designs
High Performance Embedded Computing Handbook
The VLSI Handbook
Progress in Computing, Analytics and Networking
High Performance Integrated Circuit Design

"...offers a tutorial guide to IC designers who want to move to the next level of chip design by unlocking the secrets of signal integrity." —Jake Buurma, Senior Vice President, Worldwide Research & Development, Cadence Design Systems, Inc. Covers signal integrity effects in high performance Radio Frequency (RF) IC Brings together research papers from the past few years that address the broad range of issues faced by IC designers and CAD managers now and in the future A Wiley-IEEE Press publication

A methodology for using domino logic in an ASIC design flow for graduate students, researchers, and circuit designers in industry.

The latest techniques for designing robust, high performance integrated circuits in nanoscale technologies Focusing on a new technological paradigm, this practical guide describes the interconnect-centric design methodologies that are now the major focus of nanoscale integrated circuits (ICs). High Performance Integrated Circuit Design begins by discussing the dominant role of on-chip interconnects and provides an overview of technology scaling. The book goes on to cover data signaling, power management,

synchronization, and substrate-aware design. Specific design constraints and methodologies unique to each type of interconnect are addressed. This comprehensive volume also explains the design of specialized circuits such as tapered buffers and repeaters for data signaling, voltage regulators for power management, and phase-locked loops for synchronization. This is an invaluable resource for students, researchers, and engineers working in the area of high performance ICs. Coverage includes: Technology scaling Interconnect modeling and extraction Signal propagation and delay analysis Interconnect coupling noise Global signaling Power generation Power distribution networks CAD of power networks Techniques to reduce power supply noise Power dissipation Synchronization theory and tradeoffs Synchronous system characteristics On-chip clock generation and distribution Substrate noise in mixed-signal ICs Techniques to reduce substrate noise

Over the years, the fundamentals of VLSI technology have evolved to include a wide range of topics and a broad range of practices. To encompass such a vast amount of knowledge, The VLSI Handbook focuses on the key concepts, models, and equations that enable the electrical engineer to analyze, design, and predict the behavior of very large-scale integrated circuits. It provides the most up-to-date information on IC technology you can find. Using frequent examples, the Handbook stresses the fundamental theory behind professional applications. Focusing not only on the traditional design methods, it contains all relevant sources of information and tools to assist you in performing your job. This includes software, databases, standards, seminars, conferences and more. The VLSI Handbook answers all your needs in one comprehensive volume at a level that will enlighten and refresh the knowledge of experienced engineers and educate the novice. This one-source reference keeps you current on new techniques and procedures and serves as a review for standard practice. It will be your first choice when looking for a solution.

ASIC Design and Synthesis

RTL Design using VHDL

First International Workshop, CHES'99 Worcester, MA, USA, August 12-13, 1999 Proceedings

A Systems Perspective

VLSI Design

Digital Logic Design Using Verilog

Domain-specific Design Platform for High-performance Signal Processing Circuits

he very name application-specific integrated circuit, or ASIC, con T notes an ability to provide a dense package for a highly complex design targeted at a focused, often complex solution. The ability to create customized high-performance designs has come of age, facilitated by so phisticated tools that enable designers to cope with ever-increasing de mands for added product functionality, features, and complexity. Most designers are trained in the traditional methods of approaching complex digital electronics with standard parts but have little, if any, exposure to custom or even semicustom integrated circuit design. Most see only a broad survey of IC technology. This book is targeted at the new ASIC designer who is getting ready to tackle that first ASIC design and is concerned about the unknowns that lie ahead. Economic and perfor mance considerations as well as tool capability and process fabrication quality have evolved to the point where consideration of ASIC design is now commonplace in an ever-increasing number of electronic systems designs. Engineers are now given the challenge of coping not only with new technologies but with new design methodologies that are fundamen tally necessary and advantageous to support new competitive high-tech products. Laypeople and engineers alike have marveled at the advances made over the years in electronics' complexity, performance, density, and cost. The migration of systems to modules to boards to integrated circuits clearly underscores the radical transition that the physical incarnation of electronics has undergone.

This book describes RTL design using Verilog, synthesis and timing closure for System On Chip (SOC) design blocks. It covers the complex RTL design scenarios and challenges for SOC designs and provides practical information on performance improvements in SOC, as well as Application Specific Integrated Circuit (ASIC) designs. Prototyping using modern high density Field Programmable Gate Arrays (FPGAs) is discussed in this book with the practical examples and case studies. The book discusses SOC design, performance improvement techniques, testing and system level verification, while also describing the modern Intel FPGA/XILINX FPGA architectures and their use in SOC prototyping. Further, the book covers the Synopsys Design Compiler (DC) and Prime Time (PT) commands, and how they can be used to optimize complex ASIC/SOC designs. The contents of this book will be useful to students and professionals alike.

In August of 2006, an engineering VP from one of Altera’s customers approached Misha Burich, VP of Engineering at Altera, asking for help in reliably being able to predict the cost, schedule and quality of system designs reliant on FPGA designs. At this time, I was responsible for defining the design flow requirements for the Altera design software and was tasked with investigating this further. As I worked with the customer to understand what worked and what did not work reliably in their FPGA design process, I noted that this problem was not unique to this one customer. The characteristics of the problem are shared by many Corporations that implement designs in FPGAs. The Corporation has many design teams at different locations and the success of the FPGA projects vary between the teams. There is a wide range of design experience across the teams. There is no working process for sharing design blocks between engineering teams. As I analyzed the data that I had received from hundreds of customer visits in the past, I noticed that design reuse among engineering teams was a challenge. I also noticed that many of the design teams at the same Companies and even within the same design team used different design methodologies. Altera had recently solved this problem as part of its own FPGA design software and IP development process.

This book provides insight into the practical design of VLSI circuits. It is aimed at novice VLSI designers and other enthusiasts who would like to understand VLSI design flows. Coverage includes key

concepts in CMOS digital design, design of DSP and communication blocks on FPGAs, ASIC front end and physical design, and analog and mixed signal design. The approach is designed to focus on practical implementation of key elements of the VLSI design process, in order to make the topic accessible to novices. The design concepts are demonstrated using software from Mathworks, Xilinx, Mentor Graphics, Synopsys and Cadence.

Third International Conference, CNC 2012, Chennai, India, February 24-25, 2012, Revised Selected Papers
Best Practices for Team-based Design
Intelligent Systems Design and Applications
Methods in Hardware/Software Co-Design
Tools and Techniques for High-Performance ASIC Design
High Performance Computing – HiPC 2005
High Performance ASIC Design

Explains how to use low power design in an automated design flow, and examine the design time and performance trade-offs Includes the latest tools and techniques for low power design applied in an ASIC design flow Focuses on low power in an automated design methodology, a much neglected area

This book describes simple to complex ASIC design practical scenarios using Verilog. It builds a story from the basic fundamentals of ASIC designs to advanced RTL design concepts using Verilog. Looking at current trends of miniaturization, the contents provide practical information on the issues in ASIC design and synthesis using Synopsys DC and their solution. The book explains how to write efficient RTL using Verilog and how to improve design performance. It also covers architecture design strategies, multiple clock domain designs, low-power design techniques, DFT, pre-layout STA and the overall ASIC design flow with case studies. The contents of this book will be useful to practicing hardware engineers, students, and hobbyists looking to learn about ASIC design and synthesis.

The book focuses to foster new and original research ideas and results in three broad areas: computing, analytics, and networking with its prospective applications in the various interdisciplinary domains of engineering. This is an exciting and emerging interdisciplinary area in which a wide range of theory and methodologies are being investigated and developed to tackle complex and challenging real world problems. It also provides insights into the International Conference on Computing Analytics and Networking (ICCAN 2017) which is a premier international open forum for scientists, researchers and technocrats in academia as well as in industries from different parts of the world to present, interact, and exchange the state of art of concepts, prototypes, innovative research ideas in several diversified fields. The book includes invited keynote papers and paper presentations from both academia and industry to initiate and ignite our young minds in the meadow of momentous research and thereby enrich their existing knowledge. The book aims at postgraduate students and researchers working in the discipline of Computer Science & Engineering. It will be also useful for the researchers working in the domain of electronics as it contains some hardware technologies and forthcoming communication technologies.

Discussing ASIC techniques of designing, troubleshooting and evaluating application specific integrated circuit chips, this book explores the concepts, principles and methods of high performance ASIC design. It covers the pros and cons of CAD tools, and discusses product customization.

US Black Engineer & IT
Cryptographic Hardware and Embedded Systems
A New Paradigm for Digital IC Design
Closing the Gap Between ASIC & Custom
Digital Design Techniques and Exercises
Coding and RTL Synthesis

This book highlights recent research on Intelligent Systems and Nature Inspired Computing. It presents 212 selected papers from the 18th International Conference on Intelligent Systems Design and Applications (ISDA 2018) and the 10th World Congress on Nature and Biologically Inspired Computing (NaBIC), which was held at VIT University, India. ISDA-NaBIC 2018 was a premier conference in the field of Computational Intelligence and brought together researchers, engineers and practitioners whose work involved intelligent systems and their applications in industry and the “real world.” Including contributions by authors from over 40 countries, the book offers a valuable reference guide for all researchers, students and practitioners in the fields of Computer Science and Engineering.

Over the past several decades, applications permeated by advances in digital signal processing have undergone unprecedented growth in capabilities. The editors and authors of High Performance Embedded Computing Handbook: A Systems Perspective have been

significant contributors to this field, and the principles and techniques presented in the handbook are reinforced by examples drawn from their work. The chapters cover system components found in today's HPEC systems by addressing design trade-offs, implementation options, and techniques of the trade, then solidifying the concepts with specific HPEC system examples. This approach provides a more valuable learning tool, Because readers learn about these subject areas through factual implementation cases drawn from the contributing authors' own experiences. Discussions include: Key subsystems and components Computational characteristics of high performance embedded algorithms and applications Front-end real-time processor technologies such as analog-to-digital conversion, application-specific integrated circuits, field programmable gate arrays, and intellectual property–based design Programmable HPEC systems technology, including interconnection fabrics, parallel and distributed processing, performance metrics and software architecture, and automatic code parallelization and optimization Examples of complex HPEC systems representative of actual prototype developments Application examples, including radar, communications, electro-optical, and sonar applications The handbook is organized around a canonical framework that helps readers navigate through the chapters, and it concludes with a discussion of future trends in HPEC systems. The material is covered at a level suitable for practicing engineers and HPEC computational practitioners and is easily adaptable to their own implementation requirements.

This book constitutes the refereed proceedings of the First International Workshop on Cryptographic Hardware and Embedded Systems, CHES'99, held in Worcester, MA, USA in August 1999. The 27 revised papers presented together with three invited contributions were carefully reviewed and selected from 42 submissions. The papers are organized in sections on cryptographic hardware, hardware architectures, smartcards and embedded systems, arithmetic algorithms, power attacks, true random numbers, cryptographic algorithms on FPGAs, elliptic curve implementations, new cryptographic schemes and modes of operation.

RTL Design and Verification

SystemVerilog for Hardware Description

Dual Mode Logic

Dedicated Digital Processors

Quick-Turnaround ASIC Design in VHDL