Low Power Design With High Level Power Estimation And Power Aware Synthesis

This book presents novel research techniques, algorithms, methodologies and experimental results for high level power estimation and power aware high-level synthesis. Readers will learn to apply such techniques to enable design flows resulting in shorter time to market and successful low power ASIC/FPGA design.

This book is a step-by-step tutorial on how to design a low-power, high-resolution (not less than 12 bit), and high-speed (not less than 200 MSps) integrated CMOS analog-to-digital (AD) converter, to respond to the challenge from the rapid growth of IoT. The discussion includes design techniques on both the system level and the circuit block level. In the architecture level, the power-efficient pipelined AD converter, the hybrid AD converter and the time-interleaved AD converter are described. In the circuit block level, the reference voltage buffer, the opamp, the comparator, and the calibration are presented. Readers designing low-power and high-performance AD converters won't want to miss this invaluable reference. Provides an in-depth introduction to the newest design techniques for the power-efficient, high-resolution (not less than 12 bit), and high-speed (not less than 200 MSps) AD converter; Presents three types of power-efficient architectures of the high-resolution and high-speed AD converter; Discusses the relevant circuit blocks (i.e., the reference voltage buffer, the opamp, and the

comparator) in two aspects, relaxing the requirements and improving the performance.

This self-contained book addresses the need for analysis, characterization, estimation, and optimization of the various forms of power dissipation in the presence of process variations of nano-CMOS technologies. The authors show very large-scale integration (VLSI) researchers and engineers how to minimize the different types of power consumption of digital circuits. The material deals primarily with high-level (architectural or behavioral) energy dissipation.

The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high-performance chips and portable devices. The study of power-saving design methodologies now must also include subjects such as systems on chips, embedded software, and the future of microelectronics. Low-Power Electronics Design covers all major aspects of low-power design of ICs in deep submicron technologies and addresses emerging topics related to future design. This volume explores, in individual chapters written by expert authors, the many low-power techniques born during the past decade. It also discusses the many different domains and disciplines that impact power consumption, including processors, complex circuits, software, CAD tools, and energy sources and management. The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality. They investigate nanotechnologies, optical circuits, ad hoc networks, e-textiles, as well as human powered sources

of energy. Low-Power Electronics Design delivers a complete picture of today's methods for reducing power, and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now.

Power Management in Mobile Devices

Low-Power Design Techniques and CAD Tools for Analog and RF Integrated Circuits

Low Power Design Methodologies

Low Power Design in Deep Submicron Electronics

High-Level Power Analysis and Optimization

Low Power Design with High-Level Power Estimation and Power-Aware SynthesisSpringer

Provides the only up-to-date source on the most recent advances inthis often complex and fascinating topic. The only book to be entirely devoted to clocking Clocking has become one of the most important topics in thefield of digital system design A "must have" book for advanced circuit engineers

Power consumption is a key limitation in many high-speed and high-data-rate electronic systems today, ranging from mobile telecom to portable and desktop computing systems, especially when moving to nanometer technologies. Ultra Low-Power Electronics and Design offers to the reader the unique opportunity of accessing in an easy and integrated fashion a mix of tutorial material and advanced research results, contributed by leading scientists from academia and industry, covering the most hot and up-to-date issues in the field of the design of ultra low-power devices, systems and

applications.

The power consumption of microprocessors is one of the most important challenges of high-performance chips and portable devices. In chapters drawn from Piguet's recently published Low-Power Electronics Design, this volume addresses the design of low-power microprocessors in deep submicron technologies. It provides a focused reference for specialists involved in systems-on-chips, from low-power microprocessors to DSP cores, reconfigurable processors, memories, ad-hoc networks, and embedded software. Low-Power Processors and Systems on Chips is organized into three broad sections for convenient access. The first section examines the design of digital signal processors for embedded applications and techniques for reducing dynamic and static power at the electrical and system levels. The second part describes several aspects of low-power systems on chips, including hardware and embedded software aspects, efficient data storage, networks-on-chips, and applications such as routing strategies in wireless RF sensing and actuating devices. The final section discusses embedded software issues, including details on compilers, retargetable compilers, and coverification tools. Providing detailed examinations contributed by leading experts, Low-Power Processors and Systems on Chips supplies authoritative information on how to maintain high performance while lowering power consumption in modern processors and

SoCs. It is a must-read for anyone designing modern computers or embedded systems.
Low-Power Processors and Systems on Chips
Unified low-power design flow for data-dominated multi-media and telecom applications
Semiconductor Devices and Technologies for Future Ultra Low Power Electronics
High-Performance and Low-Power Aspects
Low-Power Design of Nanometer FPGAs

A discussion of a compressed-domain approach for designing and implementing digital video coding systems, which is drastically different from the traditional hybrid approach. It demonstrates how the combination of discrete cosine transform (DCT) coders and motion compensated (MC) units reduces power consumption and hardware complexity.
Low-Power Digital VLSI Design: Circuits and Systems addresses both process technologies and device modeling. Power dissipation in CMOS circuits, several practical circuit examples, and low-power techniques are discussed. Low-voltage issues for digital CMOS and BiCMOS circuits are emphasized. The book also provides an extensive study of advanced CMOS subsystem design. A low-power design methodology is presented with various power minimization techniques at the circuit, logic, architecture and algorithm levels. Features: Low-voltage CMOS device modeling, technology files, design rules Switching activity concept, low-power guidelines to engineering practice Pass-transistor logic families Power dissipation of I/O circuits Multi- and low-VT CMOS logic, static power reduction circuit techniques State of the art design of low-voltage BiCMOS and CMOS

circuits Low-power techniques in CMOS SRAMS and DRAMS Low-power on-chip voltage down converter design Numerous advanced CMOS subsystems (e.g. adders, multipliers, data path, memories, regular structures, phase-locked loops) with several design options trading power, delay and area Low-power design methodology, power estimation techniques Power reduction techniques at the logic, architecture and algorithm levels More than 190 circuits explained at the transistor level.

This book provides a practical guide for engineers doing low power System-on-Chip (SoC) designs. It covers various aspects of low power design from architectural issues and design techniques to circuit design of power gating switches. In addition to providing a theoretical basis for these techniques, the book addresses the practical issues of implementing them in today's designs with today's tools.

This unique book provides an overview of the current state of the art and very recent research results that have been achieved as part of the Low-Power Initiative of the European Union, in the field of analogue, RF and mixed-signal design methodologies and CAD tools.

Designing CMOS Circuits for Low Power

Low-Power Cmos Vlsi Circuit Design

Devices, Circuits and Applications

Extreme Low-Power Mixed Signal IC Design

Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS

This book covers the fundamentals and significance of 2-D materials and related

semiconductor transistor technologies for the next-generation ultra low power applications. It provides comprehensive coverage on advanced low power transistors such as NCFETs, FinFETs, TFETs, and flexible transistors for future ultra low power applications owing to their better subthreshold swing and scalability. In addition, the text examines the use of field-effect transistors for biosensing applications and covers design considerations and compact modeling of advanced low power transistors such as NCFETs, FinFETs, and TFETs. TCAD simulation examples are also provided. FEATURES Discusses the latest updates in the field of ultra low power semiconductor transistors Provides both experimental and analytical solutions for TFETs and NCFETs Presents synthesis and fabrication processes for FinFETs Reviews details on 2-D materials and 2-D transistors Explores the application of FETs for biosensing in the healthcare field This book is aimed at researchers, professionals, and graduate students in electrical engineering, electronics and communication engineering, electron devices, nanoelectronics and nanotechnology, microelectronics, and solid-state circuits.

This book describes the design of CMOS

circuits for ultra-low power consumption including analog, radio frequency (RF), and digital signal processing circuits (DSP). The book addresses issues from circuit and system design to production design, and applies the ultra-low power circuits described to systems for digital hearing aids and capsule endoscope devices. Provides a valuable introduction to ultra-low power circuit design, aimed at practicing design engineers; Describes all key building blocks of ultra-low power circuits, from a systems perspective; Applies circuits and systems described to real product examples such as hearing aids and capsule endoscopes.

Chip Design and Implementation from a Practical Viewpoint Focusing on chip implementation, Low-Power NoC for High-Performance SoC Design provides practical knowledge and real examples of how to use network on chip (NoC) in the design of system on chip (SoC). It discusses many architectural and theoretical studies on NoCs, including design methodology, topology exploration, quality-of-service guarantee, low-power design, and implementation trials. The Steps to Implement NoC The book covers the full spectrum of the subject, from theory to actual chip design using NoC. Employing

the Unified Modeling Language (UML) throughout, it presents complicated concepts, such as models of computation and communication-computation partitioning, in a manner accessible to laypeople. The authors provide guidelines on how to simplify complex networking theory to design a working chip. In addition, they explore the novel NoC techniques and implementations of the Basic On-Chip Network (BONE) project. Examples of real-time decisions, circuit-level design, systems, and chips give the material a real-world context. Low-Power NoC and Its Application to SoC Design Emphasizing the application of NoC to SoC design, this book shows how to build the complicated interconnections on SoC while keeping a low power consumption.

This is the first book devoted to low power circuit design, and its authors have been among the first to publish papers in this area.· Low-Power CMOS VLSI Design· Physics of Power Dissipation in CMOS FET Devices· Power Estimation· Synthesis for Low Power· Design and Test of Low-Voltage CMOS Circuits· Low-Power Static Ram Architectures· Low-Energy Computing Using Energy Recovery Techniques· Software Design for Low Power

Practical Low Power Digital VLSI Design

Low-Power NoC for High-Performance SoC Design

Design and Modeling of Low Power VLSI Systems

Design of Digital Video Coding Systems

Low-Power Digital VLSI Design

Very Large Scale Integration (VLSI) Systems refer to the latest development in computer microchips which are created by integrating hundreds of thousands of transistors into one chip. Emerging research in this area has the potential to uncover further applications for VSLI technologies in addition to system advancements. Design and Modeling of Low Power VLSI Systems analyzes various traditional and modern low power techniques for integrated circuit design in addition to the limiting factors of existing techniques and methods for optimization. Through a research-based discussion of the technicalities involved in the VLSI hardware development process cycle, this book is a useful resource for researchers, engineers, and graduate-level students in computer science and engineering.

From ASICs to SOCs: A Practical Approach, by Farzad Nekoogar and Faranak Nekoogar, covers the techniques, principles, and everyday realities of designing ASICs and SOCs. Material includes current issues in the field, front-end and back-end designs, integration of IPs on SOC designs, and low-power design techniques and methodologies.

Appropriate for practicing chip designers as well as graduate students in electrical engineering.

Low Power Design Methodologies presents the first in-depth coverage of all the layers of the design hierarchy, ranging from the technology, circuit, logic and architectural levels, up to the system layer. The book gives insight into the mechanisms of power dissipation in digital circuits and presents state of the art approaches to power reduction. Finally, it introduces a global view of low power design methodologies and how these are being captured in the latest design automation environments. The individual chapters are written by the leading researchers in the area, drawn from both industry and academia. Extensive references are included at the end of each chapter. Audience: A broad introduction for anyone interested in low power design. Can also be used as a text book for an advanced graduate class. A starting point for any aspiring researcher.

This collection of important papers provides a comprehensive overview of low-power system design, from component technologies and circuits to architecture, system design, and CAD techniques. LOW POWER CMOS DESIGN summarizes the key low-power contributions through papers written by experts in this evolving field.

Low-Power Deep Sub-Micron CMOS Logic

Ultra Low-Power Electronics and Design

Circuits, Systems, and Applications
Circuits and Systems
High-Resolution and High-Speed Integrated CMOS AD Converters for Low-Power Applications

Low Power Design in Deep Submicron Electronics deals with the different aspects of low power design for deep submicron electronics at all levels of abstraction from system level to circuit level and technology. Its objective is to guide industrial and academic engineers and researchers in the selection of methods, technologies and tools and to provide a baseline for further developments. Furthermore the book has been written to serve as a textbook for postgraduate student courses. In order to achieve both goals, it is structured into different chapters each of which addresses a different phase of the design, a particular level of abstraction, a unique design style or technology. These design-related chapters are amended by motivations in Chapter 2, which presents visions both of future low power applications and technology advancements, and by some advanced case studies in Chapter 9. From the Foreword: `... This global nature of design for low power was well understood by Wolfgang Nebel and Jean Mermet when organizing the NATO workshop which is the origin of the book. They invited the best experts in the field to cover all aspects of low power design. As a result the chapters in this book are covering deep-submicron CMOS digital system design for low power in a systematic way from process technology all the way up to software design and embedded software systems. Low Power Design in Deep Submicron Electronics is an excellent guide for the practicing engineer, the researcher and the student interested in this crucial aspect of actual CMOS design. It contains about a thousand references to all aspects of the recent five years of feverish activity in this exciting aspect of design.' Hugo de Man Professor, K.U. Leuven, Belgium Senior Research Fellow, IMEC, Belgium

Low-Power Design of Nanometer FPGAs Architecture and EDA is an invaluable reference for researchers and practicing engineers

concerned with power-efficient, FPGA design. State-of-the-art power reduction techniques for FPGAs will be described and compared. These techniques can be applied at the circuit, architecture, and electronic design automation levels to describe both the dynamic and leakage power sources and enable strategies for codesign. Low-power techniques presented at key FPGA design levels for circuits, architectures, and electronic design automation, form critical, "bridge" guidelines for codesign Comprehensive review of leakage-tolerant techniques empowers designers to minimize power dissipation Provides valuable tools for estimating power efficiency/savings of current, low-power FPGA design techniques

1. 1 Power-dissipation trends in CMOS circuits Shrinking device geometry, growing chip area and increased data-processing speed performance are technological trends in the integrated circuit industry to enlarge chip functionality. Already in 1965 Gordon Moore predicted that the total number of devices on a chip would double every year until the 1970s and every 24 months in the 1980s. This prediction is widely known as "Moore's Law" and eventually culminated in the Semiconductor Industry Association (SIA) technology road map [1]. The SIA road map has been a guide for the in dustry leading them to continued wafer and die size growth, increased transistor density and operating frequencies, and defect density reduction. To mention a few numbers; the die size increased 7% per year, the smallest feature sizes decreased 30% and the operating frequencies doubled every two years. As a consequence of these trends both the number of transistors and the power dissi pation per unit area increase. In the near future the maximum power dissipation per unit area will be reached. Down-scaling of the supply voltage is not only the most effective way to reduce power dissipation in general it also is a necessary precondition to ensure device reliability by reducing electrical fields and device temperature, to prevent device degradation. A draw-back of this solution is an increased signal propa gation delay, which results in a lower data-processing speed performance.

The power consumption of microprocessors is one of the most

important challenges of high-performance chips and portable devices. In chapters drawn from Piguet's recently published Low-Power Electronics Design, Low-Power CMOS Circuits: Technology, Logic Design, and CAD Tools addresses the design of low-power circuitry in deep submicron technologies. It provides a focused reference for specialists involved in designing low-power circuitry, from transistors to logic gates. The book is organized into three broad sections for convenient access. The first examines the history of low-power electronics along with a look at emerging and possible future technologies. It also considers other technologies, such as nanotechnologies and optical chips, that may be useful in designing integrated circuits. The second part explains the techniques used to reduce power consumption at low levels. These include clock gating, leakage reduction, interconnecting and communication on chips, and adiabatic circuits. The final section discusses various CAD tools for designing low-power circuits. This section includes three chapters that demonstrate the tools and low-power design issues at three major companies that produce logic synthesizers. Providing detailed examinations contributed by leading experts, Low-Power CMOS Circuits: Technology, Logic Design, and CAD Tools supplies authoritative information on how to design and model for high performance with low power consumption in modern integrated circuits. It is a must-read for anyone designing modern computers or embedded systems.

Subthreshold Source-Coupled Circuits

Low Power Digital CMOS Design

Low-Power High-Level Synthesis for Nanoscale CMOS Circuits

Low Power Design Essentials

Ultra-Low Power Integrated Circuit Design

This book is the first in aseries on novellow power design architectures, methods and design practices. It results from of a large European project started in 1997, whose goal is to promote

the further development and the faster and wider industrial use of advanced design methods for reducing the power consumption of electronic systems. Low power design became crucial with the wide spread of portable information and cornrnunication terminals, where a small battery has to last for a long period. High performance electronics, in addition, suffers from a permanent increase of the dissipated power per square millimetre of silicon, due to the increasing eIock-rates, which causes cooling and reliability problems or otherwise limits the performance. The European Union's Information Technologies Programme 'Esprit' did there fore launch a 'Pilot action for Low Power Design' , wh ich eventually grew to 19 R&D projects and one coordination project, with an overall budget of 14 million Euro. It is meanwhile known as European Low Power Initiative for Electronic System Design (ESD-LPD) and will be completed by the end of 2001. It involves 30 major Euro pean companies and 20 well-known institutes. The R&D projects aims to develop or demonstrate new design methods for power reduction, while the coordination project takes care that the methods, experiences and results are properly documented and pub licised. Design exibility and power consumption in addition to the cost, have always been the most important issues in design of integrated circuits

(ICs), and are the main concerns of this research, as well. Energy Consumptions: Power dissipation (P) and energy consumption are - diss pecially importantwhen there is a limited amountof power budgetor limited source of energy. Very common examples are portable systems where the battery life time depends on system power consumption. Many different techniques have been - veloped to reduce or manage the circuit power consumption in this type of systems. Ultra-low power (ULP) applications are another examples where power dissipation is the primary design issue. In such applications, the power budget is so restricted that very special circuit and system level design techniquesare needed to satisfy the requirements. Circuits employed in applications such as wireless sensor networks (WSN), wearable battery powered systems [1], and implantable circuits for biol- ical applications need to consume very low amount of power such that the entire system can survive for a very long time without the need for changingor recharging battery[2–4]. Using newpowersupplytechniquessuchas energyharvesting[5]and printable batteries [6], is another reason for reducing power dissipation. Devel- ing special design techniques for implementing low power circuits [7–9], as well as dynamic power management (DPM) schemes [10] are the two main approaches to control the system

power consumption. Design Flexibility: Design exibility is the other important issue in modern in-grated systems.

This book describes methodologies in the design of VLSI devices, circuits and their applications at nanoscale levels. The book begins with the discussion on the dominant role of power dissipation in highly scaled devices.The 15 Chapters of the book are classified under four sections that cover design, modeling, and simulation of electronic, magnetic and compound semiconductors for their applications in VLSI devices, circuits, and systems. This comprehensive volume eloquently presents the design methodologies for ultra–low power VLSI design, potential post–CMOS devices, and their applications from the architectural and system perspectives. The book shall serve as an invaluable reference book for the graduate students, Ph.D./ M.S./ M.Tech. Scholars, researchers, and practicing engineers working in the frontier areas of nanoscale VLSI design.

Sealed Lead Acid…Nickel Cadmium…Lithium Ion… How do you balance battery life with performance and cost? This book shows you how! Now that "mobile" has become the standard, the consumer not only expects mobility but demands power longevity in wireless devices. As more and more features, computing power, and memory are

*packed into mobile devices such as iPods, cell phones, and cameras, there is a large and growing gap between what devices can do and the amount of energy engineers can deliver. In fact, the main limiting factor in many portable designs is not hardware or software, but instead how much power can be delivered to the device. This book describes various design approaches to reduce the amount of power a circuit consumes and techniques to effectively manage the available power. Power Management Advice On: •Low Power Packaging Techniques •Power and Clock Gating •Energy Efficient Compilers •Various Display Technologies •Linear vs. Switched Regulators •Software Techniques and Intelligent Algorithms * Addresses power versus performance that each newly developed mobile device faces * Robust case studies drawn from the author's 30 plus years of extensive real world experience are included * Both hardware and software are discussed concerning their roles in power*

A Complete Compressed Domain Approach

Architecture and EDA

A Practical Approach

Sub-threshold Current Reduction

Nanoscale VLSI

this book is not suitable for the bookstore catalogue

System on Chip Interfaces for Low Power Design provides a top-down understanding of interfaces available to SoC

developers, not only the underlying protocols and architecture of each, but also how they interact and the tradeoffs involved. The book offers a common context to help understand the variety of available interfaces and make sense of technology from different vendors aligned with multiple standards. With particular emphasis on power as a factor, the authors explain how each interface performs in various usage scenarios and discuss their advantages and disadvantages. Readers learn to make educated decisions on what interfaces to use when designing systems and gain insight for innovating new/custom interfaces for a subsystem and their potential impact. Provides a top-down guide to SoC interfaces for memory, multimedia, sensors, display, and communication Explores the underlying protocols and architecture of each interface with multiple examples Guides through competing standards and explains how different interfaces might interact or interfere with each other Explains challenges in system design, validation, debugging and their impact on development

This book contains all the topics of importance to the low power designer. It first lays the foundation and then goes on to detail the design process. The book also discusses such special topics as power management and modal design, ultra low power, and low power design methodology and flows. In addition, coverage includes projections of the future and case studies.

Oversampling techniques based on sigma-delta modulation are widely used to implement the analog/digital interfaces in CMOS VLSI technologies. This approach is relatively insensitive to imperfections in the manufacturing process

and offers numerous advantages for the realization of high-resolution analog-to-digital (A/D) converters in the low-voltage environment that is increasingly demanded by advanced VLSI technologies and by portable electronic systems. In The Design of Low-Voltage, Low-Power Sigma-Delta Modulators, an analysis of power dissipation in sigma-delta modulators is presented, and a low-voltage implementation of a digital-audio performance A/D converter based on the results of this analysis is described. Although significant power savings can typically be achieved in digital circuits by reducing the power supply voltage, the power dissipation in analog circuits actually tends to increase with decreasing supply voltages. Oversampling architectures are a potentially power-efficient means of implementing high-resolution A/D converters because they reduce the number and complexity of the analog circuits in comparison with Nyquist-rate converters. In fact, it is shown that the power dissipation of a sigma-delta modulator can approach that of a single integrator with the resolution and bandwidth required for a given application. In this research the influence of various parameters on the power dissipation of the modulator has been evaluated and strategies for the design of a power-efficient implementation have been identified. The Design of Low-Voltage, Low-Power Sigma-Delta Modulators begins with an overview of A/D conversion, emphasizing sigma-delta modulators. It includes a detailed analysis of noise in sigma-delta modulators, analyzes power dissipation in integrator circuits, and addresses practical issues in the circuit design and testing of a high-resolution modulator. The Design of

Low-Voltage, Low-Power Sigma-Delta Modulators will be of interest to practicing engineers and researchers in the areas of mixed-signal and analog integrated circuit design.

Low Power Design with High-Level Power Estimation and Power-Aware Synthesis

Technology, Logic Design and CAD Tools

System on Chip Interfaces for Low Power Design

Low-Power CMOS Circuits

For System-on-Chip Design

Power consumption has become a major design consideration for battery-operated, portable systems as well as high-performance, desktop systems. Strict limitations on power dissipation must be met by the designer while still meeting ever higher computational requirements. A comprehensive approach is thus required at all levels of system design, ranging from algorithms and architectures to the logic styles and the underlying technology. Potentially one of the most important techniques involves combining architecture optimization with voltage scaling, allowing a trade-off between silicon area and low-power operation. Architectural optimization enables supply voltages of the order of 1 V using standard CMOS technology. Several

techniques can also be used to minimize the switched capacitance, including representation, optimizing signal correlations, minimizing spurious transitions, optimizing sequencing of operations, activity-driven power down, etc. The high- efficiency of DC-DC converter circuitry required for efficient, low-voltage and low-current level operation is described by Stratakos, Sullivan and Sanders. The application of various low-power techniques to a chip set for multimedia applications shows that orders-of-magnitude reduction in power consumption is possible. The book also features an analysis by Professor Meindl of the fundamental limits of power consumption achievable at all levels of the design hierarchy. Svensson, of ISI, describes emerging adiabatic switching techniques that can break the CV2f barrier and reduce the energy per computation at a fixed voltage. Srivastava, of AT&T, presents the application of aggressive shut-down techniques to microprocessor applications.

This book is the fourth in a series on

novel low power design architectures, methods and design practices. It results from of a large European project started in 1997, whose goal is to promote the further development and the faster and wider industrial use of advanced design methods for reducing the power con sumption of electronic systems. Low power design became crucial with the wide spread of portable infor mation and communication terminals, where a small battery has to last for a long period. High performance electronics, in addition, suffers from a per manent increase of the dissipated power per square millimeter of silicon, due to the increasing clock-rates, which causes cooling and reliability problems or otherwise limits the performance. The European Union's Information Technologies Programme 'Esprit' did therefore launch a 'Pilot action for Low Power Design', which eventually grew to 19 R&D projects and one coordination project, with an overall budget of 14 million EURO. It is meanwhile known as European Low Power Initiative for Electronic System Design

(ESD-LPD) and will be completed in the year 2002. It involves to develop or demonstrate new design methods for power reduction, while the coordination project takes care that the methods, experiences and results are properly documented and publicised.

High-Level Power Analysis and Optimization presents a comprehensive description of power analysis and optimization techniques at the higher (architecture and behavior) levels of the design hierarchy, which are often the levels that yield the most power savings. This book describes power estimation and optimization techniques for use during high-level (behavioral synthesis), as well as for designs expressed at the register-transfer or architecture level. High-Level Power Analysis and Optimization surveys the state-of-the-art research on the following topics: power estimation/macromodeling techniques for architecture-level designs, high-level power management techniques, and high-level synthesis optimizations for low power. High-Level Power Analysis and Optimization will be very useful

reading for students, researchers, designers, design methodology developers, and EDA tool developers who are interested in low-power VLSI design or high-level design methodologies. Practical Low Power Digital VLSI Design emphasizes the optimization and trade-off techniques that involve power dissipation, in the hope that the readers are better prepared the next time they are presented with a low power design problem. The book highlights the basic principles, methodologies and techniques that are common to most CMOS digital designs. The advantages and disadvantages of a particular low power technique are discussed. Besides the classical area-performance trade-off, the impact to design cycle time, complexity, risk, testability and reusability are discussed. The wide impacts to all aspects of design are what make low power problems challenging and interesting. Heavy emphasis is given to top-down structured design style, with occasional coverage in the semicustom design methodology. The examples and design techniques cited have been known

to be applied to production scale designs or laboratory settings. The goal of Practical Low Power Digital VLSI Design is to permit the readers to practice the low power techniques using current generation design style and process technology. Practical Low Power Digital VLSI Design considers a wide range of design abstraction levels spanning circuit, logic, architecture and system. Substantial basic knowledge is provided for qualitative and quantitative analysis at the different design abstraction levels. Low power techniques are presented at the circuit, logic, architecture and system levels. Special techniques that are specific to some key areas of digital chip design are discussed as well as some of the low power techniques that are just appearing on the horizon. Practical Low Power Digital VLSI Design will be of benefit to VLSI design engineers and students who have a fundamental knowledge of CMOS digital design.

Low Power Networks-on-Chip

From ASICs to SOCs

The Design of Low-Voltage, Low-Power Sigma-Delta Modulators

Low-Power Electronics Design

In recent years, both Networks-on-Chip, as an architectural solution for high-speed interconnect, and power consumption, as a key design constraint, have continued to gain interest in the design and research communities. This book offers a single-source reference to some of the most important design techniques proposed in the context of low-power design for networks-on-chip architectures.

Based on selected partner contributions of the European Low Power Initiative for Electronic System Design of the European Community ESPRIT4 programme

Low Power Methodology Manual

Digital System Clocking

Low-Power CMOS Design

Introduction to Low-Power Design in VLSIs