

Access Free The Art Of
Hardware Architecture Design
Methods And

The Art Of Hardware Architecture Design Methods And

The purpose of this book is to evaluate strategies for future system design in multiprocessor system-on-chip (MPSoC) architectures. Both hardware design and integration of new development tools will be discussed. Novel trends in MPSoC design, combined with reconfigurable architectures are a main topic of concern. The main emphasis is on

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architectures, design-flow, tool-development, applications and system design.

Intelligent readers who want to build their own embedded computer systems-- installed in everything from cell phones to cars to handheld organizers to refrigerators-- will find this book to be the most in-depth, practical, and up-to-date guide on the market. Designing Embedded Hardware carefully steers between the practical and philosophical aspects, so developers can both create

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their own devices and gadgets and customize and extend off-the-shelf systems. There are hundreds of books to choose from if you need to learn programming, but only a few are available if you want to learn to create hardware. Designing Embedded Hardware provides software and hardware engineers with no prior experience in embedded systems with the necessary conceptual and design building blocks to understand the architectures of embedded systems. Written to

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provide the depth of coverage and real-world examples developers need, Designing Embedded Hardware also provides a road-map to the pitfalls and traps to avoid in designing embedded systems. Designing Embedded Hardware covers such essential topics as:

- The principles of developing computer hardware
- Core hardware designs
- Assembly language concepts
- Parallel I/O
- Analog-digital conversion
- Timers (internal and external)
- UART Serial Peripheral Interface Inter-

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Integrated Circuit Bus
Controller Area Network
(CAN) Data Converter
Interface (DCI) Low-power
operation This invaluable
and eminently useful book
gives you the practical
tools and skills to
develop, build, and
program your own
application-specific
computers.

80486 System Architecture
describes the hardware
architecture of PC
products using the Intel
family of 80486 chips,
providing a clear, concise
explanation of the 80486
processor's relationship

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to the rest of the system.

The author provides a comprehensive treatment of the processor including:

- 80486 microarchitecture and its functional units
 - internal and external caches
 - hardware interface
 - SL technology features
 - instructions new to the 80486
 - the register set
 - 486/487SX processors
 - 486DX2 processors
 - 486DX2 write-back enhanced processor
 - 486DX4 processors
 - implementation-specific issues
 - main memory subsystem design
 - OverDrive processors
- If you design or test

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hardware or software that involves 486 processors, 80486 System Architecture is an essential, time-saving tool. The PC System Architecture Series is a crisply written and comprehensive set of guides to the most important PC hardware standards. Each title explains from a programmer's perspective the architecture, features, and operations of systems built using one particular type of chip or hardware specification. The PC System Architecture Series features step-by-

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step descriptions and instructions and accessible illustrations that enable a wide range of readers to easily understand difficult hardware topics. The authors, expert hardware training consultants for clients including IBM, Intel, Compaq, and Dell, have mastered the art of pinpointing and succinctly explaining just the critical information that PC programmers, software and hardware designers, and engineers need to know and leaving out the rest. The result is an exciting

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series of books that will enable readers of a wide range of backgrounds to make immediate gains in programming productivity. This book presents and discusses innovative ideas in the design, modelling, implementation, and optimization of hardware platforms for neural networks. The rapid growth of server, desktop, and embedded applications based on deep learning has brought about a renaissance in interest in neural networks, with applications including image and speech

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processing, data analytics, robotics, healthcare monitoring, and IoT solutions. Efficient implementation of neural networks to support complex deep learning-based applications is a complex challenge for embedded and mobile computing platforms with limited computational/storage resources and a tight power budget. Even for cloud-scale systems it is critical to select the right hardware configuration based on the neural network complexity

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and system constraints in order to increase power- and performance-efficiency. Hardware Architectures for Deep Learning provides an overview of this new field, from principles to applications, for researchers, postgraduate students and engineers who work on learning-based services and hardware platforms.

The Genius of
Architecture, Or, The
Analogy of that Art with
Our Sensations

3D Video Coding for
Embedded Devices

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The Art of Systems
Architecting, Third
Edition

An Illustrated

Introduction to

Microprocessors and

Computer Architecture

Efficient Processing of

Deep Neural Networks

Art in Architecture

Program

Software Defined Radio makes
wireless communications easier,
more efficient, and more reliable.

This book bridges the gap between
academic research and practical
implementation. When beginning a
project, practicing engineers,
technical managers, and graduate
students can save countless hours

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by considering the concepts presented in these pages. The author covers the myriad options and trade-offs available when selecting an appropriate hardware architecture. As demonstrated here, the choice between hardware- and software-centric architecture can mean the difference between meeting an aggressive schedule and bogging down in endless design iterations. Because of the author's experience overseeing dozens of failed and successful developments, he is able to present many real-life examples. Some of the key concepts covered are: Choosing the right architecture for the market -

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laboratory, military, or commercial, Hardware platforms – FPGAs, GPPs, specialized and hybrid devices, Standardization efforts to ensure interoperability and portabilitym State-of-the-art components for radio frequency, mixed-signal, and baseband processing. The text requires only minimal knowledge of wireless communications; whenever possible, qualitative arguments are used instead of equations. An appendix provides a quick overview of wireless communications and introduces most of the concepts the readers will need to take advantage of the material. An essential introduction to SDR, this book is sure to be an

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invaluable addition to any technical bookshelf.

This book describes the most recent techniques for turbo decoder implementation, especially for 4G and beyond 4G applications. The authors reveal techniques for the design of high-throughput decoders for future telecommunication systems, enabling designers to reduce hardware cost and shorten processing time. Coverage includes an explanation of VLSI implementation of the turbo decoder, from basic functional units to advanced parallel architecture. The authors discuss both hardware architecture techniques and experimental

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results, showing the variations in area/throughput/performance with respect to several techniques. This book also illustrates turbo decoders for 3GPP-LTE/LTE-A and IEEE 802.16e/m standards, which provide a low-complexity but high-flexibility circuit structure to support these standards in multiple parallel modes. Moreover, some solutions that can overcome the limitation upon the speedup of parallel architecture by modification to turbo codec are presented here. Compared to the traditional designs, these methods can lead to at most 33% gain in throughput with similar performance and similar cost. Holger Scherl introduces the

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reader to the reconstruction problem in computed tomography and its major scientific challenges that range from computational efficiency to the fulfillment of Tuy's sufficiency condition. The assessed hardware architectures include multi- and many-core systems, cell broadband engine architecture, graphics processing units, and field programmable gate arrays.

Systems Architecture, Sixth Edition, is the most comprehensive introduction to information systems hardware and software in business. This new edition remains an indispensable tool for IS students, emphasizing a managerial, broad systems

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perspective for a holistic approach to systems architecture. Each chapter has been updated thoroughly to reflect the changing nature of new technologies, and all end-of-chapter material has been enhanced and expanded.

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Multithreaded Computer
Architecture: A Summary of the
State of the ART
Hardware Architectures for Post-
Quantum Digital Signature
Schemes
Hardware and Software Support
for Virtualization

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The Elements of Computing
Systems

On ASIC and FPGA

An Information Technology
Approach

Explores the
fundamentals required to
understand, analyze, and
implement space
modulation techniques
(SMTs) in coherent and
non-coherent radio
frequency environments

This book focuses on the
concept of space
modulation techniques
(SMTs), and covers those
emerging high data rate
wireless communication

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techniques. The book discusses the advantages and disadvantages of SMTs along with their performance. A general framework for analyzing the performance of SMTs is provided and used to detail their performance over several generalized fading channels. The book also addresses the transmitter design of these techniques with the optimum number of hardware components and the use of these techniques in cooperative and mm-Wave

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communications.

Beginning with an introduction to the subject and a brief history, Space Modulation Techniques goes on to offer chapters covering MIMO systems like spatial multiplexing and space-time coding. It then looks at channel models, such as Rayleigh, Rician, Nakagami-m, and other generalized distributions. A discussion of SMTs includes techniques like space shift keying

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(SSK), space-time shift keying (STSK), trellis coded spatial modulation (TCSM), spatial modulation (SM), generalized spatial modulation (GSM), quadrature spatial modulation (QSM), and more. The book also presents a non-coherent design for different SMTs, and a framework for SMTs' performance analysis in different channel conditions and in the presence of channel imperfections, all that along with an

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information theoretic treatment of SMTs. Lastly, it provides performance comparisons, results, and MATLAB codes and offers readers practical implementation designs for SMTs. The book also: Provides readers with the expertise of the inventors of space modulation techniques (SMTs) Analyzes error performance, capacity performance, and system complexity. Discusses practical implementation of SMTs and studies SMTs

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with cooperative and mm-Wave communications
Explores and compares MIMO schemes Space Modulation Techniques is an ideal book for professional and academic readers that are active in the field of SMT MIMO systems. If engineering is the art and science of technical problem solving, systems architecting happens when you don't yet know what the problem is. The third edition of a highly respected

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bestseller, The Art of Systems Architecting provides in-depth coverage of the least understood part of systems design: moving from a vague concept and limited resources to a satisfactory and feasible system concept and an executable program. The book provides a practical, heuristic approach to the "art" of systems architecting. It provides methods for embracing, and then taming, the growing

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complexity of modern systems. New in the Third Edition: Five major case studies illustrating successful and unsuccessful practices Information on architecture frameworks as standards for architecture descriptions New methods for integrating business strategy and architecture and the role of architecture as the technical embodiment of strategy Integration of process guidance for organizing and managing

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architecture projects
Updates to the rapidly
changing fields of
software and systems-of-
systems architecture
Organization of
heuristics around a
simple and practical
process model A
Practical Heuristic
Approach to the Art of
Systems Architecting
Extensively rewritten to
reflect the latest
developments, the text
explains how to create a
system from scratch,
presenting
invention/design rules

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together with clear explanations of how to use them. The author supplies practical guidelines for avoiding common systematic failures while implementing new mandates. He uses a heuristics-based approach that provides an organized attack on very ill-structured engineering problems. Examining architecture as more than a set of diagrams and documents, but as a set of decisions that either

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drive a system to success or doom it to failure, the book provide methods for integrating business strategy with technical architectural decision making.

This book guides readers through the design of hardware architectures using VHDL for digital communication and image processing applications that require performance computing. Further it includes the description of all the VHDL-related notions, such as

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language, levels of abstraction, combinational vs. sequential logic, structural and behavioral description, digital circuit design, and finite state machines. It also includes numerous examples to make the concepts presented in text more easily understandable.

A study of the relationship between platform and creative expression in the Atari VCS. The Atari Video

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Computer System

dominated the home video game market so completely that "Atari" became the generic term for a video game console. The Atari VCS was affordable and offered the flexibility of changeable cartridges. Nearly a thousand of these were created, the most significant of which established new techniques, mechanics, and even entire genres. This book offers a detailed and accessible

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study of this influential video game console from both computational and cultural perspectives. Studies of digital media have rarely investigated platforms—the systems underlying computing. This book (the first in a series of Platform Studies) does so, developing a critical approach that examines the relationship between platforms and creative expression. Nick Montfort and Ian Bogost discuss the Atari VCS

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itself and examine in detail six game cartridges: Combat, Adventure, Pac-Man, Yars' Revenge, Pitfall!, and Star Wars: The Empire Strikes Back. They describe the technical constraints and affordances of the system and track developments in programming, gameplay, interface, and aesthetics. Adventure, for example, was the first game to represent a virtual space larger than the screen

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(anticipating the boundless virtual spaces of such later games as World of Warcraft and Grand Theft Auto), by allowing the player to walk off one side into another space; and Star Wars: The Empire Strikes Back was an early instance of interaction between media properties and video games.

Montfort and Bogost show that the Atari VCS—often considered merely a retro fetish object—is an essential part of the history of video games.

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The Architecture of
Computer Hardware,
Systems Software, and
Networking
Computer Organization
and Design RISC-V
Edition
Aspects of Visualization
80486 System
Architecture
Hardware Design and Tool
Integration
Learning Computer
Architecture with
Raspberry Pi
*Om hvordan mikroprocessorer
fungerer, med undersøgelse
af de nyeste
mikroprocessorer fra Intel,*

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IBM og Motorola.

This book focuses on the core question of the necessary architectural support provided by hardware to efficiently run virtual machines, and of the corresponding design of the hypervisors that run them. Virtualization is still possible when the instruction set architecture lacks such support, but the hypervisor remains more complex and must rely on additional techniques. Despite the focus on architectural support in current architectures, some historical perspective is necessary to appropriately frame the problem. The first

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half of the book provides the historical perspective of the theoretical framework developed four decades ago by Popek and Goldberg. It also describes earlier systems that enabled virtualization despite the lack of architectural support in hardware. As is often the case, theory defines a necessary—but not sufficient—set of features, and modern architectures are the result of the combination of the theoretical framework with insights derived from practical systems. The second half of the book describes state-of-the-art support for virtualization

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in both x86-64 and ARM processors. This book includes an in-depth description of the CPU, memory, and I/O virtualization of these two processor architectures, as well as case studies on the Linux/KVM, VMware, and Xen hypervisors. It concludes with a performance comparison of virtualization on current-generation x86- and ARM-based systems across multiple hypervisors. This book explores C-based design, implementation, and analysis of post-quantum cryptography (PQC) algorithms for signature generation and verification. The authors investigate NIST

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round 2 PQC algorithms for signature generation and signature verification from a hardware implementation perspective, especially focusing on C-based design, power-performance-area-security (PPAS) trade-offs and design flows targeting FPGAs and ASICs. Describes a comprehensive set of synthesizable c code base as well as the hardware implementations for the different types of PQC algorithms including lattice-based, code-based, and multivariate-based; Demonstrates the hardware (FPGA and ASIC) and hardware-software optimizations and trade-offs of the NIST round

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2 signature-based PQC algorithms; Enables designers to build hardware implementations that are resilient to a variety of side-channels.

This handbook presents fundamental knowledge on the hardware/software (HW/SW) codesign methodology.

Contributing expert authors look at key techniques in the design flow as well as selected codesign tools and design environments, building on basic knowledge to consider the latest techniques. The book enables readers to gain real benefits from the HW/SW codesign methodology through explanations and case

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studies which demonstrate its usefulness. Readers are invited to follow the progress of design techniques through this work, which assists readers in following current research directions and learning about state-of-the-art techniques. Students and researchers will appreciate the wide spectrum of subjects that belong to the design methodology from this handbook.

Multiprocessor System-on-Chip

Distributed Embedded Smart Cameras

*Computer Architecture
Software Aspects, Coding,
and Hardware*

Access Free The Art Of Hardware Architecture Design Methods And *Processor and System-on-Chip Simulation Racing the Beam*

The book's aim is to highlight all the complex issues, tasks and techniques that must be mastered by a SoC Architect to define and architect SoC for an embedded application. This book is primarily focused on real problems with emphasis on architectural techniques across various aspects of chip-design, especially in context to embedded systems. The book covers aspects of embedded systems in a consistent way, starting with basic concepts that provides introduction to embedded systems and gradually increasing the depth to reach advanced concepts, such as power management and design consideration for maximum power efficiency and higher battery life. Theoretical part has been intentionally kept to the minimum that is essentially

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required to understand the subject. The guidelines explained across various chapters are independent of any CAD tool or silicon process and are applicable to any SoC architecture targeted for embedded systems.

The new RISC-V Edition of Computer Organization and Design features the RISC-V open source instruction set architecture, the first open source architecture designed to be used in modern computing environments such as cloud computing, mobile devices, and other embedded systems. With the post-PC era now upon us, Computer Organization and Design moves forward to explore this generational change with examples, exercises, and material highlighting the emergence of mobile computing and the Cloud. Updated content featuring tablet computers, Cloud infrastructure, and the x86 (cloud computing) and ARM (mobile

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computing devices) architectures is included. An online companion Web site provides advanced content for further study, appendices, glossary, references, and recommended reading. Features RISC-V, the first such architecture designed to be used in modern computing environments, such as cloud computing, mobile devices, and other embedded systems Includes relevant examples, exercises, and material highlighting the emergence of mobile computing and the cloud

With the new developments in computer architecture, fairly recent publications can quickly become outdated. Computer Architecture: Software Aspects, Coding, and Hardware takes a modern approach. This comprehensive, practical text provides that critical understanding of a central processor by clearly detailing fundamentals, and cutting edge design

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features. With its balanced software/hardware perspective and its description of Pentium processors, the book allows readers to acquire practical PC software experience. The text presents a foundation-level set of ideas, design concepts, and applications that fully meet the requirements of computer organization and architecture courses. The book features a "bottom up" computer design approach, based upon the author's thirty years experience in both academe and industry. By combining computer engineering with electrical engineering, the author describes how logic circuits are designed in a CPU. The extensive coverage of a microgrammed CPU and new processor design features gives the insight of current computer development. Computer Architecture: Software Aspects, Coding, and Hardware presents a comprehensive review of the subject, from

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beginner to advanced levels. Topics include: o Two's complement numbers o Integer overflow o Exponent overflow and underflow o Looping o Addressing modes o Indexing o Subroutine linking o I/O structures o Memory mapped I/O o Cycle stealing o Interrupts o Multitasking o Microprogrammed CPU o Multiplication tree o Instruction queue o Multimedia instructions o Instruction cache o Virtual memory o Data cache o Alpha chip o Interprocessor communications o Branch prediction o Speculative loading o Register stack o JAVA virtual machine o Stack machine principles

Use your Raspberry Pi to get smart about computing fundamentals In the 1980s, the tech revolution was kickstarted by a flood of relatively inexpensive, highly programmable computers like the Commodore. Now, a second revolution in computing is beginning with the

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Raspberry Pi. Learning Computer Architecture with the Raspberry Pi is the premier guide to understanding the components of the most exciting tech product available. Thanks to this book, every Raspberry Pi owner can understand how the computer works and how to access all of its hardware and software capabilities. Now, students, hackers, and casual users alike can discover how computers work with Learning Computer Architecture with the Raspberry Pi. This book explains what each and every hardware component does, how they relate to one another, and how they correspond to the components of other computing systems. You'll also learn how programming works and how the operating system relates to the Raspberry Pi's physical components. Co-authored by Eben Upton, one of the creators of the Raspberry Pi, this is a companion volume

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to the Raspberry Pi User Guide An affordable solution for learning about computer system design considerations and experimenting with low-level programming Understandable descriptions of the functions of memory storage, Ethernet, cameras, processors, and more Gain knowledge of computer design and operation in general by exploring the basic structure of the Raspberry Pi The Raspberry Pi was created to bring forth a new generation of computer scientists, developers, and architects who understand the inner workings of the computers that have become essential to our daily lives. Learning Computer Architecture with the Raspberry Pi is your gateway to the world of computer system design. The Atari Video Computer System Application-Specific Hardware Architecture Design with VHDL State of the Art in Computer Graphics

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Designing Embedded Hardware
Hardware Architectures for Deep Learning
Hardware and Software Perspectives

*Acquire the Design
Information, Methods, and
Skills Needed to Master the
New VLIW Architecture!*

*VLIW Microprocessor
Hardware Design offers you
a complete guide to VLIW
hardware design—providing
state-of-the-art coverage of
microarchitectures, RTL
coding, ASIC flow, and
FPGA flow of design. The
book also contains a wide
range of skills-building
examples, all worked using
Verilog, that equip you with*

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a practical, hands-on tutorial for understanding each step in the VLIW microprocessor design process. Written by Weng Fook Lee, an internationally renowned expert in the field of microprocessor design, this cutting-edge hardware design tool presents unsurpassed coverage of the latests in VLIW microprocessing. Authoritative and comprehensive, VLIW Microprocessor Hardware Design features: Step-by-step information on the VLIW hardware design

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process A wealth of Verilog-based designs ASIC and FPGA implementations Expert guidance on the best-known methods for RTL coding Over 75 detailed illustrations that clarify each aspect of VLIW design Inside this Complete VLIW Microprocessor Toolkit • Introduction • Design Methodology • RTL Coding, Testbenching, and Simulation • FPGA Implementation • Testbenches and Simulation Results • Synthesis Results and Gate Level Netlist The computing world today

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is in the middle of a revolution: mobile clients and cloud computing have emerged as the dominant paradigms driving programming and hardware innovation today. The Fifth Edition of Computer Architecture focuses on this dramatic shift, exploring the ways in which software and technology in the cloud are accessed by cell phones, tablets, laptops, and other mobile computing devices. Each chapter includes two real-world examples, one mobile and one datacenter, to illustrate this

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revolutionary change.

*Updated to cover the mobile
computing revolution*

*Emphasizes the two most
important topics in*

*architecture today: memory
hierarchy and parallelism in
all its forms. Develops*

*common themes throughout
each chapter: power,*

performance, cost,

dependability, protection,

programming models, and

emerging trends ("What's

Next") Includes three review

appendices in the printed

text. Additional reference

appendices are available

online. Includes updated

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Case Studies and completely new exercises.

State of the Art in Computer Graphics Aspects of Visualization This is the fourth volume derived from a State of . . . the Art in Computer Graphics Summer Institute. It represents a snapshot of a number of topics in computer graphics, topics which include visualization of scientific data; modeling; some aspects of visualization in virtual reality; and hardware architectures for visualization. Many papers first present a background

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introduction to the topic, followed by discussion of current work in the topic. The volume is thus equally suitable for nonspecialists in a particular area, and for the more experienced researcher in the field. It also enables general readers to obtain an acquaintance with a particular topic area sufficient to apply that knowledge in the context of solving current problems. The volume is organized into four chapters - Visualization of Data, Modeling, Virtual Reality Techniques, and Hardware Architectures for

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Visualization. In the first chapter, Val Watson and Pamela Walatka address the visual aspects of fluid dynamic computations. They discuss algorithms for function-mapped surfaces and cutting planes, isosurfaces, particle traces, and topology extractions. They point out that current visualization systems are limited by low information transfer bandwidth, poor response to viewing and model accuracy modification requests, mismatches between model rendering and human cognitive

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capabilities, and ineffective interactive tools. However, Watson and Walatka indicate that proposed systems will correct most of these problems.

This book provides a structured treatment of the key principles and techniques for enabling efficient processing of deep neural networks (DNNs).

DNNs are currently widely used for many artificial intelligence (AI)

applications, including computer vision, speech recognition, and robotics.

While DNNs deliver state-of-

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the-art accuracy on many AI tasks, it comes at the cost of high computational complexity. Therefore, techniques that enable efficient processing of deep neural networks to improve metrics—such as energy-efficiency, throughput, and latency—without sacrificing accuracy or increasing hardware costs are critical to enabling the wide deployment of DNNs in AI systems. The book includes background on DNN processing; a description and taxonomy of hardware architectural approaches for

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*designing DNN accelerators;
key metrics for evaluating
and comparing different
designs; features of the
DNN processing that are
amenable to
hardware/algorithm co-
design to improve energy
efficiency and throughput;
and opportunities for
applying new technologies.
Readers will find a
structured introduction to
the field as well as a
formalization and
organization of key concepts
from contemporary works
that provides insights that
may spark new ideas.*

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*Evaluation of State-of-the-
Art Hardware Architectures
for Fast Cone-Beam CT*

Reconstruction

Parallel Computer

Architecture

A Quantitative Approach

Heterogeneous Computing

The Art of Hardware

Architecture

Building a Modern

Computer from First

Principles

**Simulation of computer
architectures has made rapid
progress recently. The primary
application areas are
hardware/software performance
estimation and optimization as well
as functional and timing**

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verification. Recent, innovative technologies such as retargetable simulator generation, dynamic binary translation, or sampling simulation have enabled widespread use of processor and system-on-chip (SoC) simulation tools in the semiconductor and embedded system industries. Simultaneously, processor and SoC simulation is still a very active research area, e.g. what amounts to higher simulation speed, flexibility, and accuracy/speed trade-offs. This book presents and discusses the principle technologies and state-of-the-art in high-level hardware architecture simulation, both at the processor and the system-on-chip level.

Multithreaded computer architecture has emerged as one of

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the most promising and exciting avenues for the exploitation of parallelism. This new field represents the confluence of several independent research directions which have united over a common set of issues and techniques. Multithreading draws on recent advances in dataflow, RISC, compiling for fine-grained parallel execution, and dynamic resource management. It offers the hope of dramatic performance increases through parallel execution for a broad spectrum of significant applications based on extensions to 'traditional' approaches. Multithreaded Computer Architecture is divided into four parts, reflecting four major perspectives on the topic. Part I provides the reader with basic

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background information, definitions, and surveys of work which have in one way or another been pivotal in defining and shaping multithreading as an architectural discipline. Part II examines key elements of multithreading, highlighting the fundamental nature of latency and synchronization. This section presents clever techniques for hiding latency and supporting large synchronization name spaces. Part III looks at three major multithreaded systems, considering issues of machine organization and compilation strategy. Part IV concludes the volume with an analysis of multithreaded architectures, showcasing methodologies and actual measurements. Multithreaded

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Computer Architecture: A Summary of the State of the Art is an excellent reference source and may be used as a text for advanced courses on the subject.

This book describes the current state of the art in big-data analytics, from a technology and hardware architecture perspective. The presentation is designed to be accessible to a broad audience, with general knowledge of hardware design and some interest in big-data analytics. Coverage includes emerging technology and devices for data-analytics, circuit design for data-analytics, and architecture and algorithms to support data-analytics. Readers will benefit from the realistic context used by the authors, which demonstrates what works, what doesn't work, and

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what are the fundamental problems, solutions, upcoming challenges and opportunities. Provides a single-source reference to hardware architectures for big-data analytics; Covers various levels of big-data analytics hardware design abstraction and flow, from device, to circuits and systems; Demonstrates how non-volatile memory (NVM) based hardware platforms can be a viable solution to existing challenges in hardware architecture for big-data analytics. If you look around you will find that all computer systems, from your portable devices to the strongest supercomputers, are heterogeneous in nature. The most obvious heterogeneity is the existence of computing nodes of different capabilities (e.g. multicore,

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GPUs, FPGAs, ...). But there are also other heterogeneity factors that exist in computing systems, like the memory system components, interconnection, etc. The main reason for these different types of heterogeneity is to have good performance with power efficiency. Heterogeneous computing results in both challenges and opportunities. This book discusses both. It shows that we need to deal with these challenges at all levels of the computing stack: from algorithms all the way to process technology. We discuss the topic of heterogeneous computing from different angles: hardware challenges, current hardware state-of-the-art, software issues, how to make the best use of the current

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heterogeneous systems, and what lies ahead. The aim of this book is to introduce the big picture of heterogeneous computing. Whether you are a hardware designer or a software developer, you need to know how the pieces of the puzzle fit together. The main goal is to bring researchers and engineers to the forefront of the research frontier in the new era that started a few years ago and is expected to continue for decades. We believe that academics, researchers, practitioners, and students will benefit from this book and will be prepared to tackle the big wave of heterogeneous computing that is here to stay.

**The Hardware Software Interface
Inside the Machine
Introduction to Soc System**

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Architecture

Embedded System Design

Handbook of Hardware/Software

Codesign

Implementing Software Defined Radio

This book highlights the complex issues, tasks and skills that must be mastered by an IP designer, in order to design an optimized and robust digital circuit to solve a problem. The techniques and methodologies described can serve as a bridge between specifications that are known to the

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designer and RTL code that is final outcome, reducing significantly the time it takes to convert initial ideas and concepts into right-first-time silicon.

Coverage focuses on real problems rather than theoretical concepts, with an emphasis on design techniques across various aspects of chip-design.

The Art of Hardware
Architecture Design
Methods and Techniques
for Digital
Circuits Springer Science

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& Business Media

This series offers a range of heretofore unavailable writings in English translation on the subjects of art, architecture, and aesthetics. Camus's description of the French hotel argues that architecture should please the senses and the mind.

This publication addresses distributed embedded smart cameras -cameras that perform on board analysis and collaborate with other

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cameras. This book provides the material required to better understand the architectural design challenges of embedded smart camera systems, the hardware/software ecosystem, the design approach for and applications of distributed smart cameras together with the state-of-the-art algorithms. The authors concentrate on the architecture, hardware/software design, realization of

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smart camera networks
from applications to
architectures, in
particular in the
embedded and mobile
domains.

Design Methods and
Techniques for Digital
Circuits

Space Modulation
Techniques

Systems Architecture
Emerging Technology and
Architecture for Big-
data Analytics

Architectures, Design
and Applications

**This book outlines a set of
issues that are critical to all of**

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architecture--communication latency, communication bandwidth, and coordination of cooperative work (across modern designs). It describes the set of techniques available in hardware and in software to address each issues and explore how the various techniques interact.

Computer Architecture: A Quantitative Approach, Sixth Edition has been considered essential reading by instructors, students and practitioners of computer design for over 20 years. The sixth edition of this classic textbook from Hennessy and

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Patterson, winners of the 2017 ACM A.M. Turing Award recognizing contributions of lasting and major technical importance to the computing field, is fully revised with the latest developments in processor and system architecture. The text now features examples from the RISC-V (RISC Five) instruction set architecture, a modern RISC instruction set developed and designed to be a free and openly adoptable standard. It also includes a new chapter on domain-specific architectures and an updated chapter on warehouse-scale computing that features the first public

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information on Google's newest WSC. True to its original mission of demystifying computer architecture, this edition continues the longstanding tradition of focusing on areas where the most exciting computing innovation is happening, while always keeping an emphasis on good engineering design. Winner of a 2019 Textbook Excellence Award (Texty) from the Textbook and Academic Authors Association Includes a new chapter on domain-specific architectures, explaining how they are the only path forward for

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improved performance and energy efficiency given the end of Moore's Law and Dennard scaling Features the first publication of several DSAs from industry Features extensive updates to the chapter on warehouse-scale computing, with the first public information on the newest Google WSC Offers updates to other chapters including new material dealing with the use of stacked DRAM; data on the performance of new NVIDIA Pascal GPU vs. new AVX-512 Intel Skylake CPU; and extensive additions to content covering multicore architecture and organization

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Includes "Putting It All Together" sections near the end of every chapter, providing real-world technology examples that demonstrate the principles covered in each chapter

Includes review appendices in the printed text and additional reference appendices available online

Includes updated and improved case studies and exercises

ACM named John L. Hennessy and David A. Patterson, recipients of the 2017 ACM A.M. Turing Award for pioneering a systematic, quantitative approach to the design and evaluation of computer architectures with

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enduring impact on the microprocessor industry. This book shows readers how to develop energy-efficient algorithms and hardware architectures to enable high-definition 3D video coding on resource-constrained embedded devices. Users of the Multiview Video Coding (MVC) standard face the challenge of exploiting its 3D video-specific coding tools for increasing compression efficiency at the cost of increasing computational complexity and, consequently, the energy consumption. This book enables readers to reduce the multiview video

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coding energy consumption through jointly considering the algorithmic and architectural levels. Coverage includes an introduction to 3D videos and an extensive discussion of the current state-of-the-art of 3D video coding, as well as energy-efficient algorithms for 3D video coding and energy-efficient hardware architecture for 3D video coding.

Architecture Design for Soft Errors provides a comprehensive description of the architectural techniques to tackle the soft error problem. It covers the new methodologies for quantitative

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analysis of soft errors as well as novel, cost-effective architectural techniques to mitigate them. To provide readers with a better grasp of the broader problem definition and solution space, this book also delves into the physics of soft errors and reviews current circuit and software mitigation techniques. There are a number of different ways this book can be read or used in a course: as a complete course on architecture design for soft errors covering the entire book; a short course on architecture design for soft errors; and as a reference book on classical fault-tolerant

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machines. This book is recommended for practitioners in semi-conductor industry, researchers and developers in computer architecture, advanced graduate seminar courses on soft errors, and (iv) as a reference book for undergraduate courses in computer architecture. Helps readers build-in fault tolerance to the billions of microchips produced each year, all of which are subject to soft errors Shows readers how to quantify their soft error reliability Provides state-of-the-art techniques to protect against soft errors
Architecture Design for Soft

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Turbo Decoder Architecture
for Beyond-4G Applications

Architectural Hardware

A Hardware/software

Approach

VLIW Microprocessor

Hardware Design

Energy Efficient Algorithms
and Architectures

The Architecture of Computer

Hardware, Systems Software and

Networking is designed help students

majoring in information technology

(IT) and information systems (IS)

understand the structure and operation

of computers and computer-based

devices. Requiring only basic computer

skills, this accessible textbook

introduces the basic principles of

system architecture and explores

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current technological practices and trends using clear, easy-to-understand language. Throughout the text, numerous relatable examples, subject-specific illustrations, and in-depth case studies reinforce key learning points and show students how important concepts are applied in the real world. This fully-updated sixth edition features a wealth of new and revised content that reflects today's technological landscape. Organized into five parts, the book first explains the role of the computer in information systems and provides an overview of its components. Subsequent sections discuss the representation of data in the computer, hardware architecture and operational concepts, the basics of computer networking, system software and operating systems, and various interconnected systems and

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components. Students are introduced to the material using ideas already familiar to them, allowing them to gradually build upon what they have learned without being overwhelmed and develop a deeper knowledge of computer architecture.

This title gives students an integrated and rigorous picture of applied computer science, as it comes to play in the construction of a simple yet powerful computer system.