Vlsi Physical Design From Graph Partitioning To Timing Closure

Practical Problems in VLSI Physical Design Automation contains problems and solutions related to various well-known algorithms used in VLSI physical design automation. Dr. Lim believes that the best way to learn new algorithms is to walk through a small example by hand. This knowledge will greatly help understand, analyze, and improve some of the well-known algorithms. The author has designed and taught a graduate-level course on physical CAD for VLSI at Georgia Tech. Over the years he has written his homework with such a focus and has maintained typeset version of the solutions.

Covers the statistical analysis and optimization issues arising due to increased process variations in current technologies. Comprises a valuable reference for statistical analysis and optimization techniques in current and future VLSI design for CAD-Tool developers and for researchers interested in starting work in this very active area of research. Written by author who lead much research in this area who provide novel ideas and approaches to handle the addressed issues Based on the authors' expansive collection of notes taken over the years, Nano-CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing, manufacturability, and yield. This innovative book covers: process technology, including sub-wavelength optical lithography; impact of process scaling on circuit and physical implementation and

low power with leaky transistors; and DFM, yield, and the impact of physical implementation.
This book covers advanced techniques in modern circuit placement. It details all of most recent placement techniques

available in the field and analyzes the optimality of these techniques. Coverage includes all the academic placement tools that competed against one another on the same industrial benchmark circuits at the International Symposium on

Physical Design (ISPD), these techniques are also extensively being used in industrial tools as well. The book provides significant amounts of analysis on each technique such as trade-offs between quality-of-results (QoR) and runtime.

Machine Learning in VLSI Computer-Aided Design

ICDSMLA 2019

Modern Circuit Placement

A Comprehensive Guide

Timing

VLSI Physical Design Automation
The fourth edition of CMOS Digital Integrated Circuits: Analysis and Design continues the well-established tradition of the earlier editions by offering the most comprehensive coverage of digital CMOS circuit design, as well as

addressing state-of-the-art technology issues highlighted by the widespread use of nanometer-scale CMOS technologies. In this latest edition, virtually all chapters have been re-written, the transistor model equations and device parameters have been revised to reflect the sigificant changes that must be taken into account for new technology generations, and the material has been reinforced with up-to-date examples. The broad-ranging coverage of this textbook starts with the fundamentals of CMOS process technology, and continues with MOS transistor models, basic CMOS gates, interconnect effects, dynamic circuits, memory circuits, arithmetic building blocks, clock and I/O circuits, low power design techniques, design for manufacturability and design for

testability.
Algorithms for VLSI Physical Design Automation is a core reference text for graduate students and CAD professionals. It provides a comprehensive treatment of the principles and algorithms of VLSI physical

design. Algorithms for VLSI Physical Design Automation presents the concepts and algorithms in an intuitive manner. Each chapter contains 3-4 algorithms that are discussed in detail. Additional algorithms are presented in a somewhat shorter format. References to advanced algorithms are presented at the end of each chapter. Algorithms for VLSI Physical Design Automation covers all aspects of physical design. The first three chapters provide the background material while the subsequent chapters focus on each phase of the physical design cycle. In addition, newer topics like physical design automation of FPGAs and MCMs have been included. The author provides an extensive bibliography which is useful for finding advanced material on a topic. Algorithms for VLSI Physical Design Automation is an invaluable reference for professionals in layout, design automation and physical design. Market_Desc: · Electrical Engineering Students taking courses on VLSI systems, CAD tools for VLSI, Design Automation at Final Year or Graduate Level, Computer Science courses on the same topics, at a similar level · Practicing Engineers wishing to learn the state of the art in VLSI Design Automation · Designers of CAD tools for chip design in software houses or large electronics companies. Special Features: · Probably the first book on Design Automation for VLSI Systems which covers all stages of design from layout synthesis through logic synthesis to high-level synthesis · Clear, precise presentation of examples, well illustrated with over 200 figures · Focus on algorithms for VLSI design tools means it will appeal to some Computer Science as well as Electrical Engineering departments About The Book: Enrollments in VLSI design automation courses are not large but it's a very popular elective, especially for those seeking a career in the microelectronics industry. Already the reviewers seem very enthusiastic about the coverage of the book being a better match for their courses than available competitors, because it covers all design phases. It has plenty of worked problems and a large no. of illustrations. It's a good 'list-builder' title that matches our strategy of focusing on topics that lie on the interface between Elec Eng and Computer

Science.

This book is intended to gather recent studies on particle swarm optimization (PSO). In this book, readers can find the recent theoretical developments and applications on PSO algorithm. From the theoretical aspect, PSO has preserved its popularity because of the fast convergence rate, and a lot of hybrid algorithms have recently been developed in order to increase the performance of the algorithm. At the same time, PSO has also been used to solve different kinds of engineering optimization problems. In this book, a reader can find engineering applications of PSO, such as environmental economic dispatch and grid computing.

Complexity Issues in VLSI

Static Timing Analysis for Nanometer Designs

On Optimal Interconnections for VLSI
Nano-CMOS Circuit and Physical Design
Top-Down Digital VLSI Design
ALGORITHMS VLSI DESIGN AUTOMATION
Presenting a comprehensive

overview of the design automation algorithms, tools, and methodologies used to design integrated circuits, the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes. The second volume, EDA for IC Implementation, Circuit

Design, and Process Technology, thoroughly examines real-time logic to GDSII (a file format used to transfer data of semiconductor physical layout), analog/mixed signal design, physical verification, and technology CAD (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability at the nanoscale, power supply network design and analysis, design modeling, and much more. Save on the complete set.

Statistical timing analysis is an area of growing importance in nanometer te- nologies, as the uncertainties associated with process and environmental var- tions increase, and this chapter has captured some of the major efforts in this area. This remains a very active field of research, and there is likely to be a great deal of new research to be found in conferences and journals after this book is published. In addition to the statistical analysis of combinational circuits, a good deal of work has been carried out in analyzing the effect of variations on clock skew. Although we will not treat this

subject in this book, the reader is referred to [LNPS00, HN01, JH01, ABZ03a] for details. 7 TIMING ANALYSIS FOR SEQUENTIAL CIRCUITS 7.1 INTRODUCTION A general sequential circuit is a network of computational nodes (gates) and memory elements

(registers). The computational nodes may be conceptualized as being clustered together in an acyclic network of gates that forms a c- binational logic circuit. A cyclic path in the direction of signal propagation 1 is permitted in the sequential circuit only if it contains at least one register . In general, it is possible to represent any sequential circuit in terms of the schematic shown in Figure 7.1, which has I inputs, O outputs and M registers. The registers outputs feed into the combinational logic which, in turn, feeds the register inputs. Thus, the combinational logic has I + M inputs and O + M outputs.

Arranged in a format that follows the industry-common ASIC physical design flow, Physical Design Essentials begins with general concepts of an ASIC library, then examines floorplanning, placement, routing, verification, and finally, testing. Among the topics covered are Basic standard cell design, transistor-sizing, and layout styles; Linear, non-linear, and polynomial characterization; Physical design constraints and floorplanning

styles; Algorithms used for placement; Clock Tree Synthesis; Parasitic extraction; Electronic Testing, and many more.
Genetic Algorithms mimic the natural process of evolution, helping engineers optimize their designs by using the principle of

"survival of the fittest". VLSI is especially suited to benefit from genetic algorithms- and this comprehensive book shows how to get the best results. You will discover how genetic algorithms work and how you can use them in a wide variety of VLSI design,

layout and test automation tasks.
VLSI Physical Design: From Graph Partitioning to Timing Closure
A Survey
An Introduction to VLSI Physical Design
EDA for IC Implementation, Circuit Design, and Process Technology

Statistical Analysis and Optimization for VLSI: Timing and Power
Genetic Algorithms: For Vlsi Design, Layout & Test Automation
This book provides a comprehensive overview of the VLSI design process. It covers end-to-end system on chip

(SoC) design, including design methodology, the design environment, tools, choice of design components, handoff procedures, and design infrastructure needs. The book also offers critical guidance on the latest UPF-based low power design flow issues for deep submicron SOC

designs, which will prepare readers for the challenges of working at the nanotechnology scale. This practical guide will provide engineers who aspire to be VLSI designers with the techniques and tools of the trade, and will also be a valuable professional reference for those already working in

VLSI design and verification with a focus on complex SoC designs. A comprehensive practical guide for VLSI designers; Covers end-to-end VLSI SoC design flow; Includes source code, case studies, and application examples.

Proceedings of a workshop which aims

to integrate theory and applications, and to find out mechanisms, concepts or tools which facilitate the implementation of solutions based on graphs. Numerous applications are covered.
&Quot;VLSI Physical Design Automation: Theory and Practice is an

essential introduction for senior undergraduates, postgraduates and anyone starting work in the field of CAD for VLSI. It covers all aspects of physical design, together with such related areas as automatic cell generation, silicon compilation, layout editors and compaction. A problem-

solving approach is adopted and each solution is illustrated with examples. Each topic is treated in a standard format: Problem Definition, Cost Functions and Constraints, Possible Approaches and Latest Developments."--BOOK JACKET.
In the last few decades, multiscale

algorithms have become a dominant trend in large-scale scientific computation. Researchers have successfully applied these methods to a wide range of simulation and optimization problems. This book gives a general overview of multiscale algorithms; applications to general *combinatorial optimization problems such as graph partitioning and the traveling salesman problem; and VLSICAD applications, including circuit partitioning, placement, and VLSI routing. Additional chapters discuss optimization in reconfigurable computing, convergence in multilevel* *optimization, and model problems with PDE constraints. Audience: Written at the graduate level, the book is intended for engineers and mathematical and computational scientists studying large-scale optimization in electronic design automation.*

Using the Electric VLSI Design System
Digital Integrated Circuit Design
FPGA Design Automation
Handbook of Algorithms for Physical Design Automation
An ASIC Design Implementation Perspective
A Practical Approach to VLSI System

on Chip (SoC) Design
This book provides readers with an up-to-date account of the use of machine learning frameworks, methodologies, algorithms and techniques in the

context of computer-aided design (CAD) for very-large-scale integrated circuits (VLSI). Coverage includes the various machine learning methods used in lithography, *physical design, yield prediction, post-silicon performance analysis, reliability and failure analysis, power and thermal analysis, analog design, logic synthesis,* *verification, and neuromorphic design. Provides up-to-date information on machine learning in VLSI CAD for device modeling, layout verifications, yield* *prediction, post-silicon validation, and reliability; Discusses the use of machine learning techniques in the context of analog and digital synthesis; Demonstrates* *how to formulate VLSI CAD objectives as machine learning problems and provides a comprehensive treatment of their efficient solutions; Discusses the tradeoff* *between the cost of collecting data and prediction accuracy and provides a methodology for using prior data to reduce cost of data collection in the design, testing and* *validation of both analog and digital VLSI designs. From the Foreword As the semiconductor industry embraces the rising swell of cognitive systems and edge intelligence, this* *book could serve as a harbinger and example of the osmosis that will exist between our cognitive structures and methods, on the one hand, and the hardware* *architectures and technologies that will support them, on the other....As we transition from the computing era to the cognitive one, it behooves us to remember* *the success story of VLSI CAD and to earnestly seek the help of the invisible hand so that our future cognitive systems are used to design more powerful cognitive systems. This* *book is very much aligned with this on-going transition from computing to cognition, and it is with deep pleasure that I recommend it to all those who are actively engaged* *in this exciting transformation. Dr. Ruchir Puri, IBM Fellow, IBM Watson CTO & Chief Architect, IBM T. J. Watson Research Center Design and optimization of* *integrated circuits are essential to the creation of new semiconductor chips, and physical optimizations are becoming more prominent as a result of semiconductor scaling.*

Modern chip design has become so complex that it is largely performed by specialized software, which is frequently updated to address advances in semiconductor *technologies and increased problem complexities. A user of such software needs a high-level understanding of the underlying mathematical models and algorithms. On* *the other hand, a developer of such software must have a keen understanding of computer science aspects, including algorithmic performance bottlenecks and how* *various algorithms operate and interact. "VLSI Physical Design: From Graph Partitioning to Timing Closure" introduces and compares algorithms that are used during the* *physical design phase of integrated-circuit design, wherein a geometric chip layout is produced starting from an abstract circuit design. The emphasis is on essential*

and fundamental techniques, ranging from hypergraph partitioning and circuit placement to timing closure.
Low-Power Digital VLSI Design: Circuits and

Systems addresses both process technologies and device modeling. Power dissipation in CMOS circuits, several practical circuit examples, and low-power *techniques are discussed. Low-voltage issues for digital CMOS and BiCMOS circuits are emphasized. The book also provides an extensive study of advanced CMOS subsystem* *design. A low-power design methodology is presented with various power minimization techniques at the circuit, logic, architecture and algorithm levels. Features: Low-*

voltage CMOS device modeling, technology files, design rules Switching activity concept, low-power guidelines to engineering practice Pass-transistor *logic families Power dissipation of I/O circuits Multi- and low-VT CMOS logic, static power reduction circuit techniques State of the art design of low-voltage*

BiCMOS and CMOS circuits Low-power techniques in CMOS SRAMS and DRAMS Low-power on-chip voltage down converter design Numerous advanced CMOS subsystems (e.g. adders, multipliers, *data path, memories, regular structures, phase-locked loops) with several design options trading power, delay and area Low-power design methodology, power estimation* *techniques Power reduction techniques at the logic, architecture and algorithm levels More than 190 circuits explained at the transistor level.*

One of Springer's renowned

Major Reference Works, this awesome achievement provides a comprehensive set of solutions to important algorithmic problems for students and researchers interested in *quickly locating useful information. This first edition of the reference focuses on high-impact solutions from the most recent decade, while later editions will widen the* *scope of the work. All entries have been written by experts, while links to Internet sites that outline their research work are provided. The entries have all been peer-*

reviewed. This defining reference is published both in print and on line.
Algorithms and Data Structures in VLSI Design
Practical Problems in VLSI Physical Design Automation

Advanced Logic Synthesis Analysis and Design Algorithms for VLSI Physical Design Automation 15th International Workshop WG '89, Castle Rolduc, The Netherlands,

June 14-16, 1989, Proceedings
The physical design flow of any project depends upon the size of the design, the technology, the number of designers, the clock frequency, and the time to

do the design. As technology advances and design-styles change, physical design flows are constantly reinvented as traditional phases are removed and new ones are added to accommodate changes in

technology. Handbook of Algorithms for Physical Design Automation provides a detailed overview of VLSI physical design automation, emphasizing state-of-the-art techniques, trends and improvements that have

emerged during the previous decade. After a brief introduction to the modern physical design problem, basic algorithmic techniques, and partitioning, the book discusses significant

advances in floorplanning representations and describes recent formulations of the floorplanning problem. The text also addresses issues of placement, net layout and optimization, routing

multiple signal nets, manufacturability, physical synthesis, special nets, and designing for specialized technologies. It includes a personal perspective from Ralph Otten as he looks back on the major technical

milestones in the history of physical design automation. Although several books on this topic are currently available, most are either too broad or out of date. Alternatively, proceedings and journal articles are

valuable resources for researchers in this area, but the material is widely dispersed in the literature. This handbook pulls together a broad variety of perspectives on the most challenging problems in the

field, and focuses on emerging problems and research results.
The Complete, Modern Tutorial on Practical VLSI Chip Design, Validation, and Analysis As microelectronics engineers design complex

chips using existing circuit libraries, they must ensure correct logical, physical, and electrical properties, and prepare for reliable foundry fabrication. VLSI Design Methodology Development focuses on the

design and analysis steps needed to perform these tasks and successfully complete a modern chip design. Microprocessor design authority Tom Dillinger carefully introduces core concepts,

and then guides engineers through modeling, functional design validation, design implementation, electrical analysis, and release to manufacturing. Writing from the engineer's perspective, he covers underlying EDA

tool algorithms, flows, criteria for assessing project status, and key tradeoffs and interdependencies. This fresh and accessible tutorial will be valuable to all VLSI system designers,

senior undergraduate or graduate students of microelectronics design, and companies offering internal courses for engineers at all levels. Reflect complexity, cost, resources, and schedules in planning a chip

design project Perform hierarchical design decomposition, floorplanning, and physical integration, addressing DFT, DFM, and DFY requirements Model functionality and behavior, validate designs,

and verify formal equivalency Apply EDA tools for logic synthesis, placement, and routing Analyze timing, noise, power, and electrical issues Prepare for manufacturing release and bring-up, from

mastering ECOs to qualification This guide is for all VLSI system designers, senior undergraduate or graduate students of microelectronics design, and companies offering internal courses

for engineers at all levels. It is applicable to engineering teams undertaking new projects and migrating existing designs to new technologies.
This book solves several mathematical problems in the

areas of Very Large Scale Integration (VLSI) and parallel computation. In particular, it describes optimal layouts for the shuffle-exchange graph, one of the best known networks for parallel computation.

Attempts to design a shuffle-exchange computer have been hampered in part by the fact that, until now, no good layouts for the shuffle-exchange graph were known.The mesh of trees network (which may

eventually prove as useful as the shuffle-exchange graph) is introduced and the book shows how it can be used to perform a variety of computations, including sorting and matrix multiplication, in a

logarithmic number of steps.Next, the book introduces the tree of meshes, the first planar graph that was discovered not to have a linear-area layout. Most recently, the structure of this graph has

been used to develop a general framework for solving VLSI graph layout problems.Finally, the book develops techniques for proving lower bounds on the bisection width, crossing number, and layout area of a

graph. These techniques significantly extend the power and range of previous methods.Researchers in the fields of VLSI, parallel computation, and graph theory will find this study of particular value; it is

also accessible to anyone with an elementary knowledge of mathematics and computer science. The book is self-contained and presents in a unified and original manner many results scattered in the technical literature,

while also covering new and fundamental results for the first time.Tom Leighton is Assistant Professor of Mathematics in the Department of Applied Mathematics and Laboratory for Computer Science at MIT.

Top-Down VLSI Design: From Architectures to Gate-Level Circuits and FPGAs represents a unique approach to learning digital design. Developed from more than 20 years teaching circuit design, Doctor Kaeslin's

approach follows the natural VLSI design flow and makes circuit design accessible for professionals with a background in systems engineering or digital signal processing. It begins with hardware architecture

and promotes a system-level view, first considering the type of intended application and letting that guide your design choices. Doctor Kaeslin presents modern considerations for handling circuit complexity,

throughput, and energy efficiency while preserving functionality. The book focuses on application-specific integrated circuits (ASICs), which along with FPGAs are increasingly used to develop products with

applications in telecommunications, IT security, biomedical, automotive, and computer vision industries. Topics include field-programmable logic, algorithms, verification, modeling

hardware, synchronous clocking, and more. Demonstrates a top-down approach to digital VLSI design. Provides a systematic overview of architecture optimization techniques. Features a

chapter on field-programmable logic devices, their technologies and architectures. Includes checklists, hints, and warnings for various design situations. Emphasizes design flows that do not

overlook important action items and which include alternative options when planning the development of microelectronic circuits.
Synthesis, Verification, and Test
A Practical Approach

Best Practices and Results
Computer Aids for VLSI Design
VLSI Design Methodology Development
VLSI Design and EDA Tools
The complexity of modern chip design requires

extensive use of specialized software throughout the process. To achieve the best results, a user of this software needs a high-level understanding of the underlying mathematical models and algorithms. In addition, a developer of such software must have a keen understanding of relevant computer science aspects, including algorithmic performance bottlenecks and how various algorithms operate and interact. This book introduces and compares the fundamental algorithms that are used during the

IC physical design phase, wherein a geometric chip layout is produced starting from an abstract circuit design. This updated second edition includes recent advancements in the state-of-the-art of physical design, and builds upon foundational coverage of essential and fundamental techniques. Numerous examples and tasks with solutions increase the clarity of presentation and facilitate deeper understanding. A comprehensive set of slides is available on the Internet for each chapter, simplifying use of the book in instructional settings. “This improved, second edition of the book will continue to serve the EDA and design community well. It is a foundational text and reference for the next generation of professionals who will be called on to continue the advancement of our chip design tools and design the most advanced microelectronics." Dr. Leon Stok, Vice President, Electronic Design Automation, IBM Systems Group "This is the book I wish I had when I taught EDA in the past, and the one I'm using from now on." Dr. Louis K. Scheffer, Howard Hughes Medical Institute "I would happily use this book when teaching Physical Design. I know of no other work

that’s as comprehensive and up-to-date, with algorithmic focus and clear pseudocode for the key algorithms. The book is beautifully designed!”
Prof. John P. Hayes,

University of Michigan
“The entire field of electronic design automation owes the authors a great debt for providing a single coherent source on

physical design that is clear and tutorial in nature, while providing details on key state-of-the-art topics such as timing closure.” Prof. Kurt Keutzer, University

of California, Berkeley
"An excellent balance of the basics and more advanced concepts, presented by top experts in the field." Prof. Sachin Sapatnekar,

University of Minnesota
The second edition of VLSI Design is a comprehensive textbook designed for undergraduate students of electrical, electronics, and electronics and

communication engineering. It provides a thorough understanding of the fundamental concepts and design of VLSI systems.
FPGA Design Automation: A Survey is an up-to-date

comprehensive survey/tutorial of FPGA design automation, with an emphasis on the recent developments within the past 5 to 10 years. The focus is on the theory and techniques that have been, or most likely will be, reduced to practice. It covers all major steps in FPGA design flow: routing and placement, circuit clustering, technology mapping and architecture-specific optimization, physical synthesis, RT-level and behavior-level synthesis, and power optimization. FPGA Design Automation: A Survey can be used as both a guide for beginners who are embarking on research in this relatively young yet exciting area, and a useful reference for established researchers in this field.

The last decade has brought explosive growth in the technology for manufac turing integrated circuits. Integrated circuits with several hundred thousand transistors are now commonplace. This manufacturing capability, combined with the economic benefits of large electronic systems, is forcing a revolution in the design of these systems and providing a challenge to those people in terested in integrated system design. Modern circuits are too complex for an individual to comprehend completely. Managing tremendous complexity and automating the design process have become crucial issues. Two groups are interested in dealing with complexity and in developing algorithms to automate the design process. One group is composed of practi tioners in computer-aided design (CAD) who develop computer programs to aid the circuit-design process. The second group is made up of computer scientists and mathemati'::~l\ns who are interested in the design and analysis of efficient combinatorial aJ::,orithms. These two groups have developed separate bodies of literature and, until recently, have had relatively little interaction. An obstacle to bringing these two groups together is the lack of books that discuss issues of importance to both groups in the same context. There are many instances when a familiarity with the literature of the other group would be beneficial. Some practitioners could use known theoretical results to improve their "cut and try" heuristics. In other cases, theoreticians have published impractical or highly abstracted toy formulations, thinking that the latter are important for circuit layout.

Proceedings of the 1st International Conference on Data Science, Machine Learning and Applications

CMOS Digital Integrated Circuits
VLSI Design
Combinatorial Algorithms for Integrated Circuit Layout
Encyclopedia of Algorithms

Multilevel Optimization in VLSICAD

One of the main problems in chip design is the enormous number of possible combinations of individual chip elements within a system, and the problem of their

compatibility. The recent application of data structures, efficient algorithms, and ordered binary decision diagrams (OBDDs) has proven vital in designing the computer chips of tomorrow. This book provides an introduction to the foundations of this interdisciplinary research area, emphasizing its applications in computer aided circuit design. This textbook, originally published in 1987, broadly examines the software required to design electronic circuitry, including integrated circuits. Topics include synthesis and analysis tools, graphics and user interface, memory representation, and more. The book also describes a real system called "Electric."

iming, timing, timing! That is the main concern of a digital designer charged with designing a semiconductor chip. What is it, how is it T described, and how does one verify it? The design team of a large digital design may

spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, the t- ing closure is the major milestone which dictates when a chip can be - leased to the semiconductor

foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex

nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis. Unfortunately, there is no book currently ava- able that can be used by a working engineer to get acquainted with the - tails of static timing analysis. The chip designers lack a central reference for information on timing, that covers the basics to the advanced timing veri- cation procedures and techniques.

On Optimal Interconnections for VLSI describes, from a geometric perspective, algorithms for high-performance, high-density interconnections during the global and detailed routing phases of circuit layout. First, the book addresses area minimization, with a focus on near-optimal approximation algorithms for minimum-cost Steiner routing. In addition to practical implementations of recent methods, the implications of recent results on spanning tree degree bounds and the method of Zelikovsky are discussed. Second, the book addresses delay minimization, starting with a discussion of accurate, yet algorithmically tractable, delay models. Recent minimum-delay constructions are highlighted, including provably good cost-radius tradeoffs, critical-sink routing algorithms, Elmore delay-optimal routing, graph Steiner arborescences, non-tree routing, and wiresizing. Third, the book addresses skew minimization for clock routing and prescribed-delay routing formulations. The discussion starts with early matching-based constructions and goes on to treat zero-skew routing with provably minimum wirelength, as well as planar clock routing. Finally, the book concludes with a discussion of multiple (competing) objectives, i.e., how to optimize area, delay, skew, and other objectives simultaneously. These techniques are useful when the routing instance has heterogeneous resources or is highly congested, as in FPGA routing, multi-chip packaging, and very dense layouts. Throughout the book, the emphasis is on practical algorithms and a complete self-contained development. On Optimal Interconnections for VLSI will be of use to both circuit designers (CAD tool users) as well as researchers and developers in

the area of performance-driven physical design.
Low-Power Digital VLSI Design
Electronic Design Automation
Optimal Layouts for the Shuffle-Exchange Graph and Other Networks

Particle Swarm Optimization with Applications

From Architectures to Gate-Level Circuits and FPGAs

Theory and Practice

This book gathers selected high-impact articles from the 1st

International Conference on Data Science, Machine Learning & Applications 2019. It highlights the latest developments in the areas of Artificial Intelligence, Machine Learning, Soft Computing, Human–Computer Interaction and various data science & machine

learning applications. It brings together scientists and researchers from different universities and industries around the world to showcase a broad range of perspectives, practices and technical expertise.
Top-down approach to practical, tool-independent, digital circuit design,

reflecting how circuits are designed. This book provides a single-source reference to the state-of-the-art in logic synthesis. Readers will benefit from the authors' expert perspectives on new technologies and logic synthesis, new data structures, big data and logic synthesis, and convergent logic synthesis. The authors describe techniques that will enable readers to take advantage of recent advances in big data techniques and frameworks in order to have better logic synthesis algorithms.

Aimed primarily for undergraduate students pursuing courses in VLSI design, the book emphasizes the physical understanding of underlying principles of the subject. It not only focuses on circuit design process obeying VLSI rules but also on technological aspects of Fabrication. VHDL modeling is discussed as the design engineer is expected to have good knowledge of it. Various Modeling issues of VLSI devices are focused which includes necessary device physics to the required level. With such an in-depth coverage and practical approach practising engineers can also use this as ready reference.

Graph-Theoretic Concepts in Computer Science
From VLSI Architectures to CMOS Fabrication
Circuits and Systems
Physical Design Essentials
OBDD - Foundations and Applications
This book provides broad and

comprehensive coverage of the entire EDA flow. EDA/VLSI practitioners and researchers in need of fluency in an "adjacent" field will find this an invaluable reference to the basic EDA concepts, principles, data structures, algorithms, and architectures for the design, verification, and test of VLSI circuits. Anyone who needs to learn the concepts, principles, data structures, algorithms, and architectures of the EDA flow will benefit from this book. Covers complete spectrum of the EDA flow, from ESL design modeling to logic/test synthesis, verification, physical design, and test - helps EDA newcomers to get "up-and-running" quickly Includes comprehensive coverage of EDA concepts, principles, data structures, algorithms, and architectures - helps all readers improve their VLSI design competence Contains latest advancements not yet available in other books, including Test compression, ESL design modeling, large-scale floorplanning, placement, routing, synthesis of clock and power/ground networks - helps readers to design/develop testable chips or products Includes industry best-practices wherever appropriate in most chapters - helps readers avoid costly mistakes